Data Sheet, DS4, March 2001

VIP, VIP-8
Versatile ISDN Port
PEB 20590 Version 2.1
PEB 20591 Version 2.1

Wired Communications

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PEB 20590, PEB 20591
PRELIMINARY

Revision History:	**2001-03-01**	DS4
Previous Version:	01.00	

Page	Subjects (major changes since last revision)
Page 15	Pull-ups for the signals TMS, TDI, TRST
Page 34	ID-Code for TAP controller
Page 29	Maximum wander tolerance
Page 35	VIP version register
Page 46	Primary inductance for recommended S/T transformer
Page 46	External S/T Receiver Circuitry
Page 38-Page 45	Electrical Characteristics
	Note: This revision history is not 100% complete.

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Preface

This document provides reference information on VIP[1] (Versatile ISDN Port).

Organization of this Document

This Data Sheet is divided into 9 chapters. It is organized as follows:

- **Chapter 1, Introduction**
  Gives a general description of the VIP, lists the key features, and presents some typical applications.

- **Chapter 2, Pin Description**
  Lists pin locations with associated signals, categorizes signals according to function, and describes signals.

- **Chapter 3, Interface Description**
  Describes the VIP external interfaces.

- **Chapter 4, Operational Description**
  Describes the VIP operations reset, initialization, analog test loops and the monitoring of illegal code violations.

- **Chapter 5, Electrical Characteristics**
  Contains the DC and AC specification and timing diagrams.

- **Chapter 6, Application Hints**
  Provides information on external line interface circuitry in U_{PN} and S/T mode, such as transformers and line protection.

- **Chapter 7, Package Outlines**

- **Chapter 8, Glossary**

- **Chapter 9, Index**

[1] Throughout this document the name VIP will be used to refer to both chip versions PEB 20590 and PEB 20591.

PRELIMINARY

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Please provide in the subject of your e-mail:
device name (VIP), device number (PEB 20590), device version (Version 2.1),

and in the body of your e-mail:
document type (Data Sheet), issue date (2001-03-01) and document revision number (DS4).

Related Documentation

- Data Sheet for DELIC Version 2.3 or higher (PEB 20570, PEB 20571)

1 Introduction

This chapter gives a general overview of the VIP including a top-level block diagram and the logic symbol diagram, it lists the key features, and presents some typical applications.

1.1 Overview

VIP (Versatile ISDN Port) is a highly-integrated multiple layer-1 transceiver IC connecting to

- U_{PN} subscriber line interfaces (2-wire) and
- S/T subscriber or trunk line interfaces (4-wire).

VIP integrates the complete analog line interface circuitry as well as the transceiver logic required for eight full-duplex channels.

Typical VIP applications include PBX line cards (U_{PN}, S/T or mixed), and small PBXs.

VIP must be operated in combination with DELIC[1)], which is required for configuration and control/activation of VIP's layer-1 transceivers. The communication path between the DELIC and the VIP is the serial IOM-2000 interface with a data rate of up to 12.288 Mbit/s. DELIC also processes the signaling information of each VIP channel by providing a dedicated HDLC controller per subscriber. For more information on DELIC and the IOM-2000 interface, please refer to the DELIC-LC/-PB Data Sheet.

1) Infineon Technologies DELIC: DSP Embedded Line and Port Interface Controller. The DELIC is available in two versions: PEB 20570 and PEB 20571.

The VIP is available in two different versions, which differ in the possible interface combinations:

Table 1 VIP Product Family

Device		Available Interfaces
VIP	PEB 20590	Four channels are programmable to either S/T or U_{PN} mode, and the other four channels can be operated in U_{PN} mode only.
VIP-8	PEB 20591	All eight channels are programmable to either S/T or U_{PN} mode.

Four channels are programmable to either S/T or U_{PN} mode, and the other four channels can be operated in U_{PN} mode only.

	Maximum Number of U_{PN} and S/T channels								
U_{PN}	8	7	6	5	4	3	2	1	0
S/T	0	1	2	3	4	4	4	4	4

All eight channels are programmable to either S/T or U_{PN} mode.

	Maximum Number of U_{PN} and S/T channels								
U_{PN}	8	7	6	5	4	3	2	1	0
S/T	0	1	2	3	4	5	6	7	8

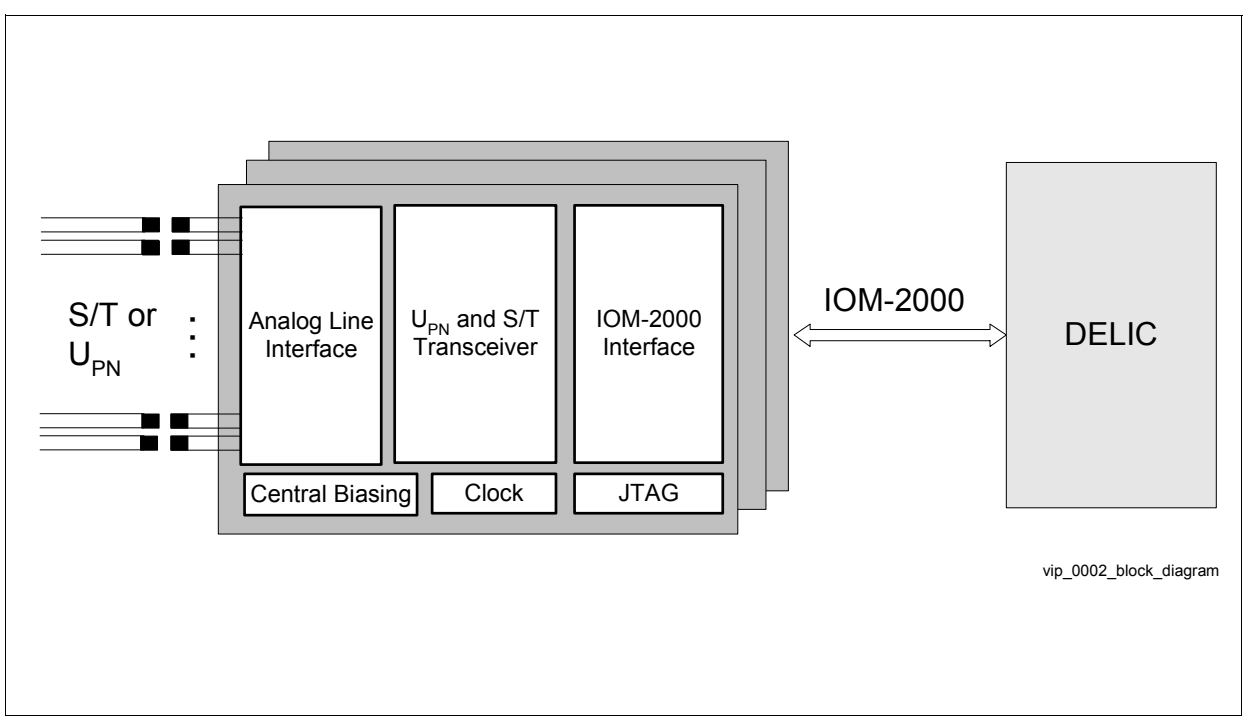
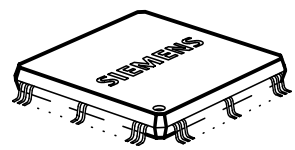


Figure 1 Top-Level Block Diagram of the VIP

1.2 VIP Key Features



P-MQFP-80-1

VIP is a universal ISDN transceiver IC for different interface modes (S/T or U_{PN}).

- Eight 2B+D line interfaces with full duplex transceivers
  - S/T interfaces at 192 kbit/s with line transceivers according to ITU-T I.430, ETSI 300.012 and ANSI T1.605
  - U_{PN} interfaces at 384 kbit/s with line transceivers according to ZVEI standard
  - Receive timing recovery
  - Conversion between pseudo-ternary and binary codes
  - Conversion between U_{PN} or S/T frames and IOM-2000 frame structures
  - Execution of test loops
  - Frame alignment in trunk applications with maximum wander correction of ± 25 µs
  - U_{PN} interface compatible to OCTAT-P (PEB 2096)[1)]
  - S/T interface compatible to QUAT-S (PEB 2084)[2)]
- IOM-2000 interface to DELIC supporting up to three VIPs (24 channels)
  - Transceiver initialization and configuration
  - Control of layer-1 activation/deactivation
  - Exchange of command and status information
- Signaling control for all VIP channels by dedicated HDLC controllers in DELIC
- Single 3.3 V power supply
- JTAG IEEE1149.1-compliant test interface with dedicated reset input

Note: U_{PN} refers to a version of the U_{P0} interface (meeting the ZVEI standard) with a reduced loop length of up to 1.3 km, depending on the type of cable.

1) Infineon Technologies OCTAT-P (PEB 2096): Octal Transceiver for U_{PN}-Interfaces.
2) Infineon Technologies QUAT-S (PEB 2084): Quadruple Transceiver for S/T-Interface.

Type	Package
PEB 20590, PEB 20591	P-MQFP-80-1

1.3 Logic Symbol Diagrams

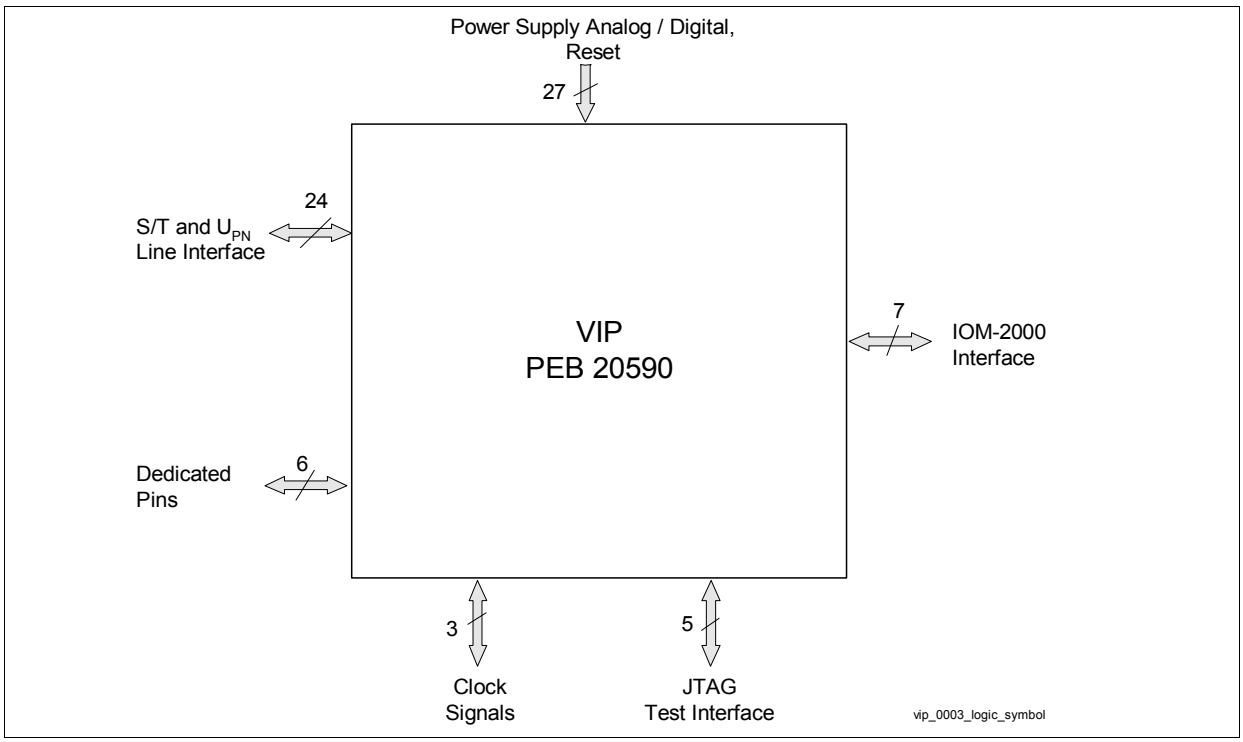


Figure 2 Logic Symbol PEB 20590 (72 of 80 Pins used)

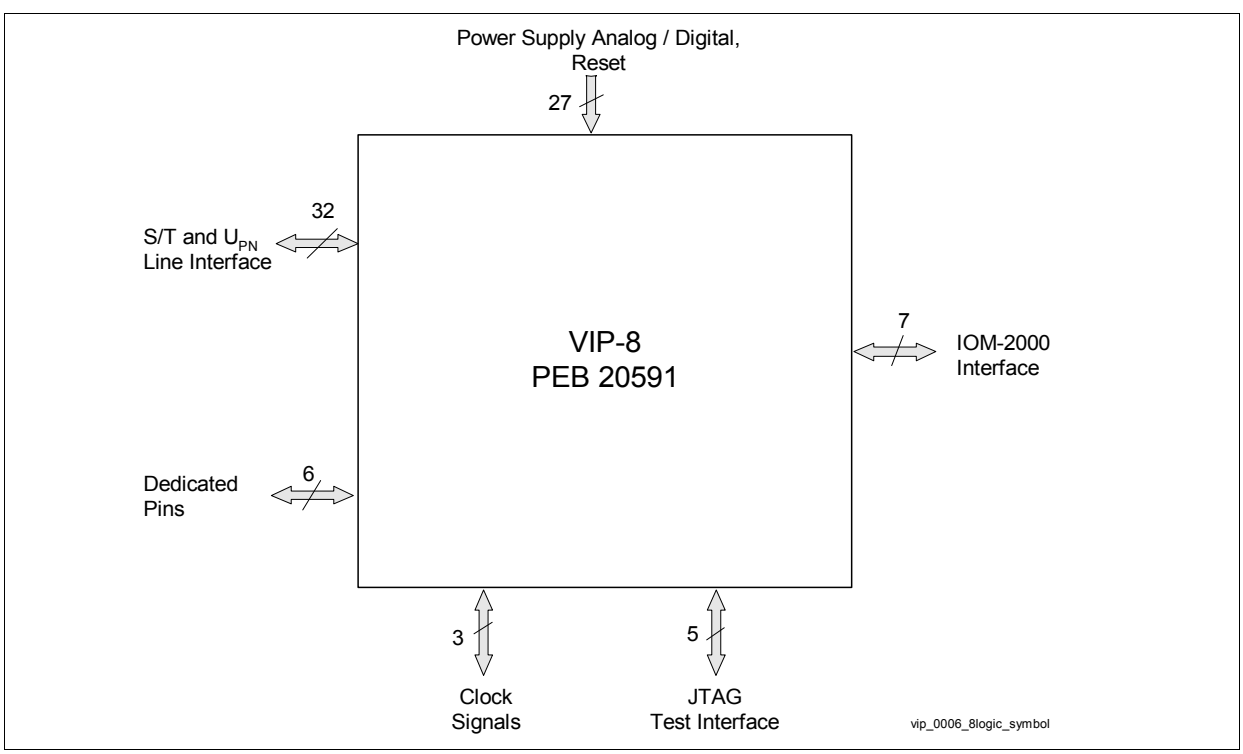


Figure 3 Logic Symbol PEB 20591

1.4 Typical Applications

Typical VIP applications are PBX line cards (U_{PN}, S/T or mixed), and small PBXs.

The following figures illustrate sample configurations in which the VIP shows its flexibility.

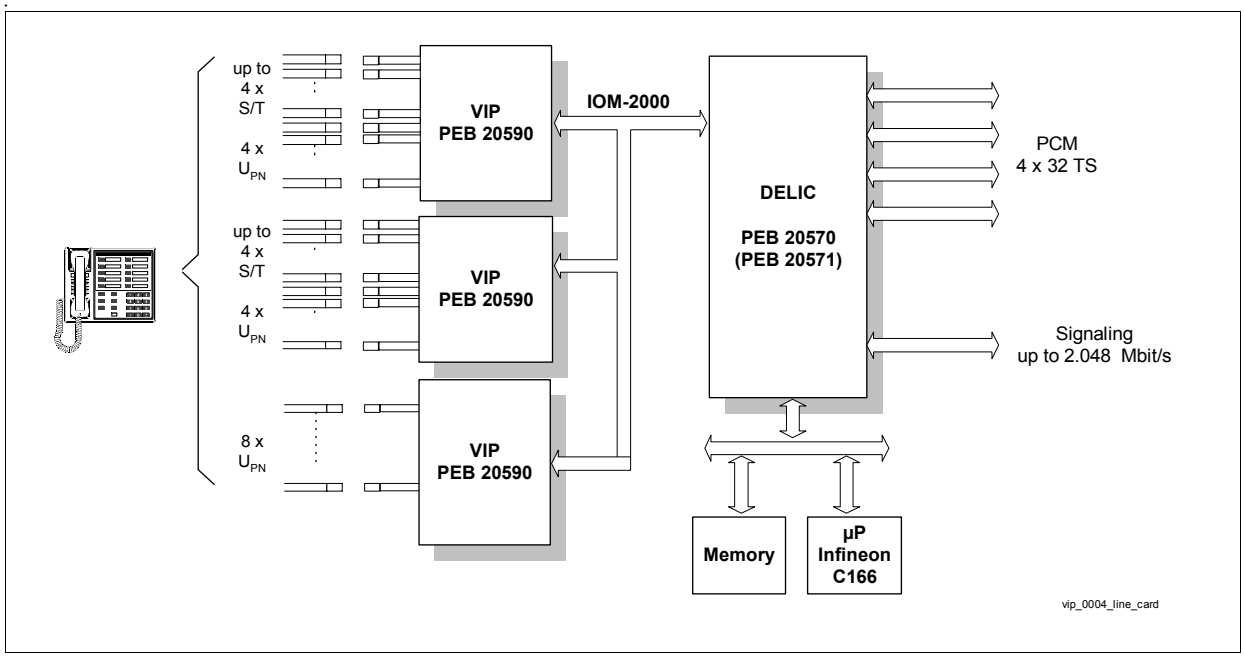


Figure 4 VIP in Mixed S/T and U_{PN} Line Cards (e.g. 8 S/T and 16 U_{PN})

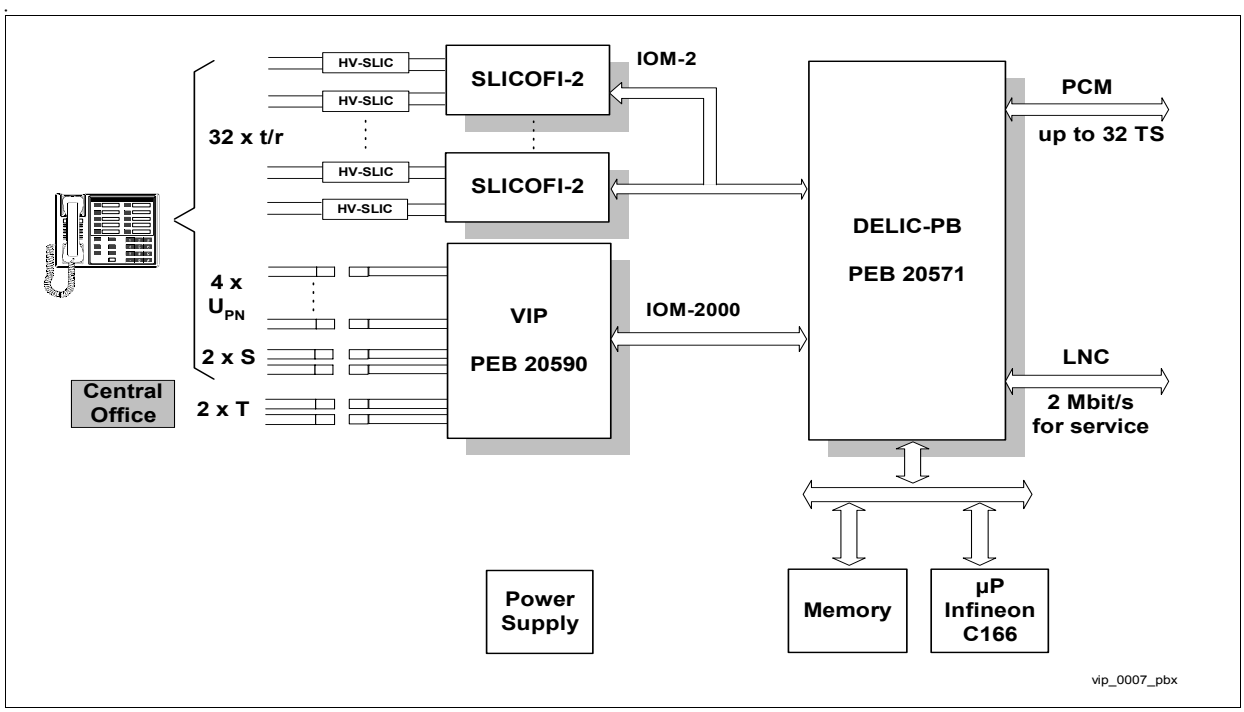


Figure 5 VIP in a Small PBX Solution

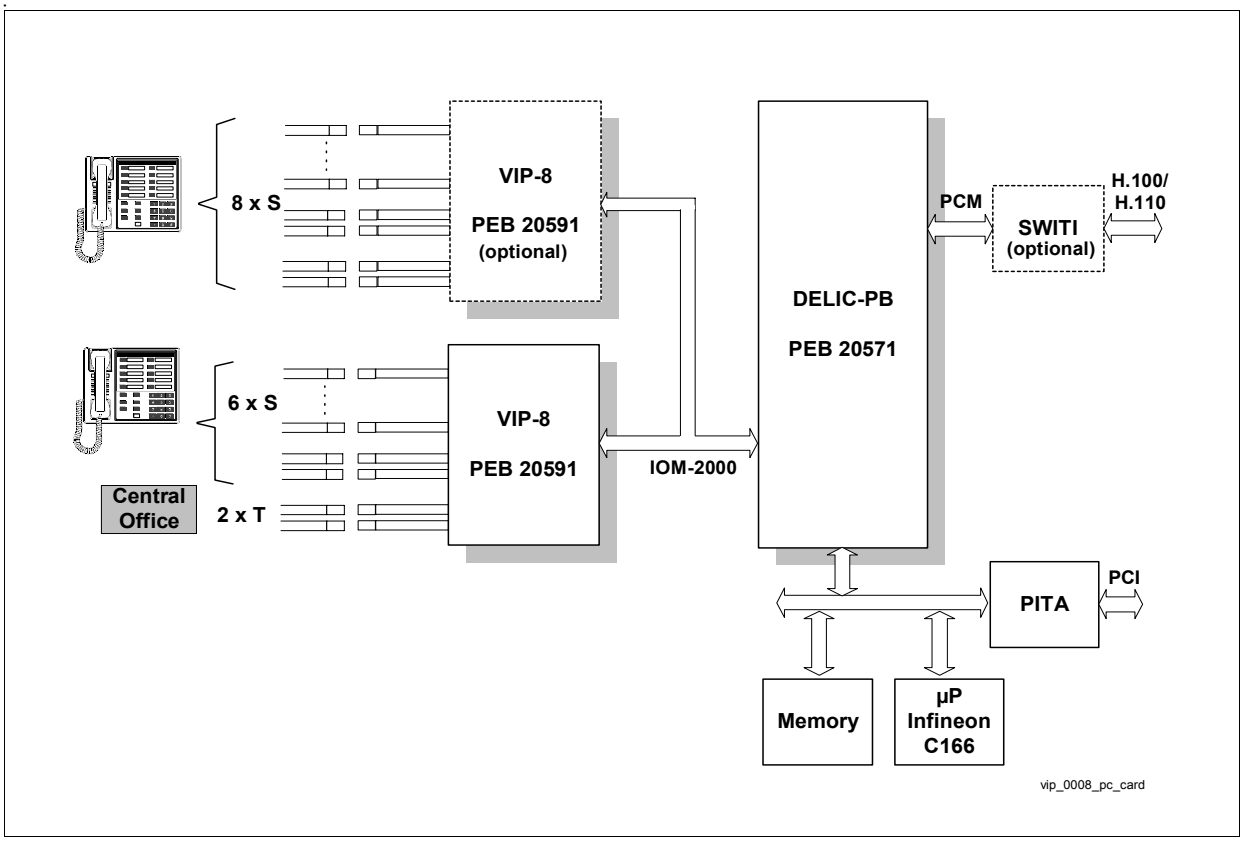


Figure 6 DELIC-PB and VIP in a PC Card for 8/16 S/T Interfaces

2 Pin Description

The VIP is available in an 80-pin Plastic Metric Quad Flat Package (P-MQFP-80-1). This chapter presents a simple layout of the 80-pin MQFP package with pin and signal callouts and a table of signal definitions.

2.1 Pin Configuration

(top view)

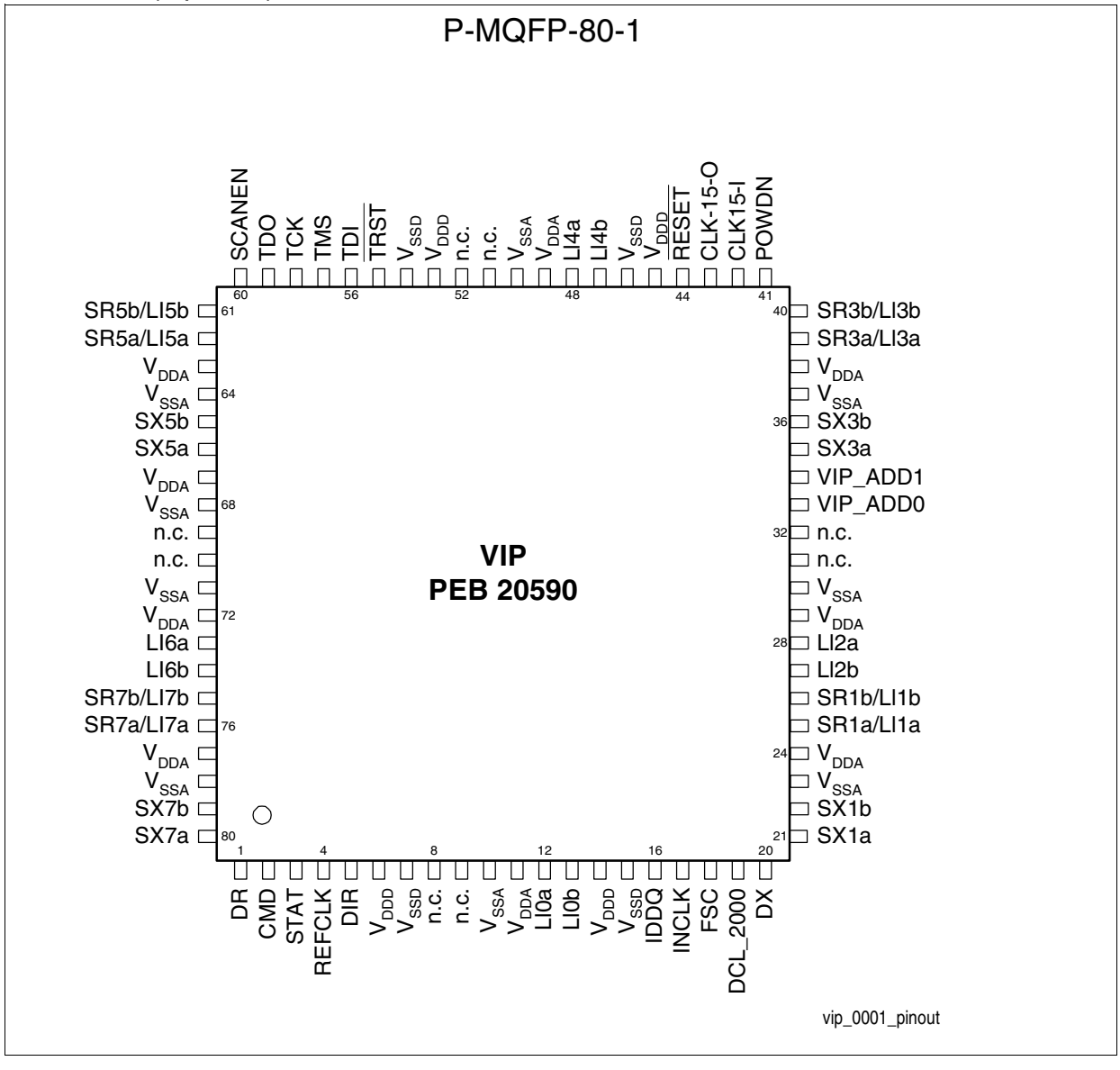


Figure 7 Pin Diagram, PEB 20590

(top view)

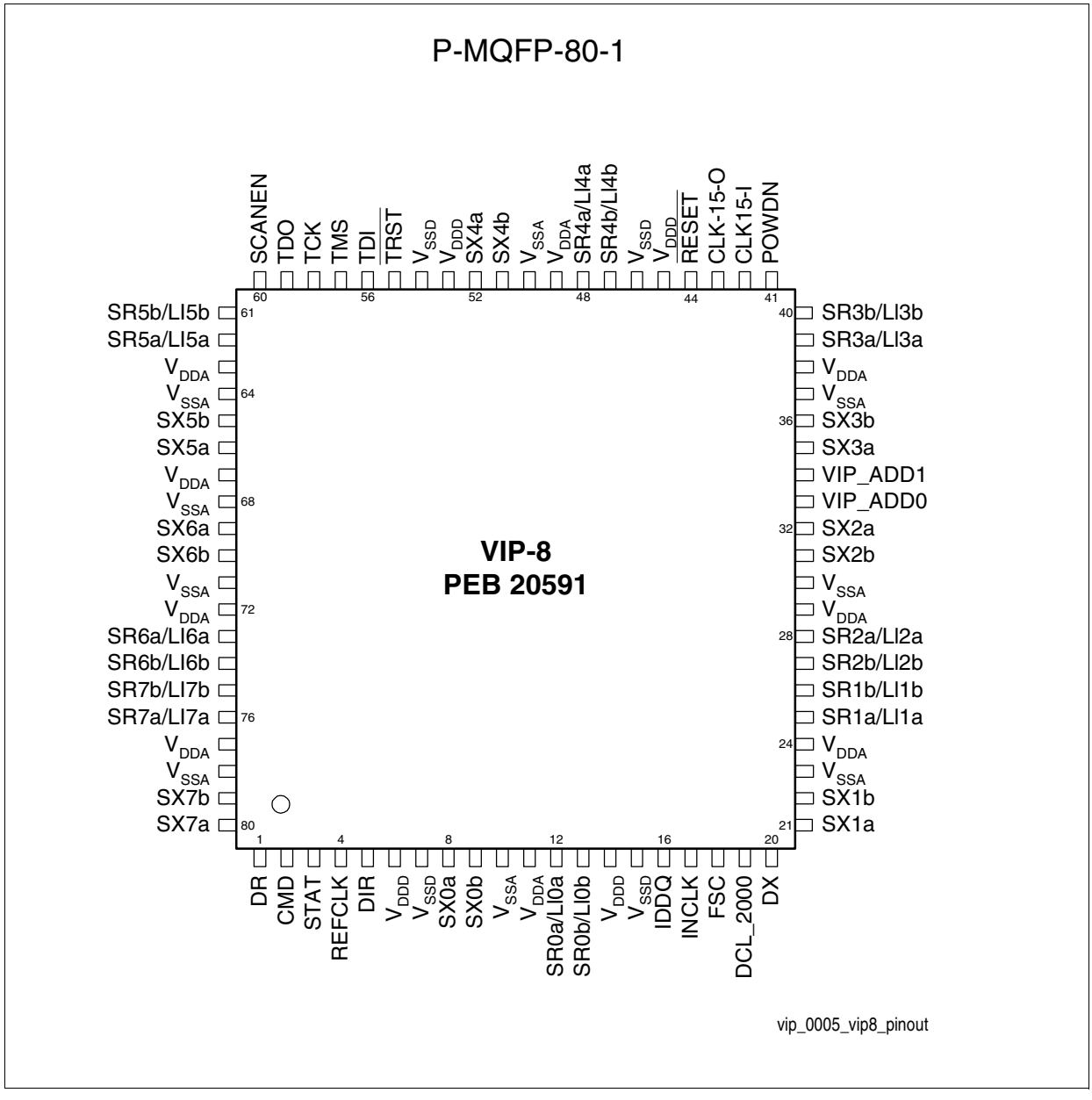


Figure 8 Pin Diagram, PEB 20591

2.2 Pin Descriptions

Table 2 PEB 20590: U_{PN} and S/T Line Interface

Pin No.	Symbol	In (I) Out(O)	During Reset	Function
25 26 39 40 62 61 76 75	SR1a/LI1a SR1b/LI1b SR3a/LI3a SR3b/LI3b SR5a/LI5a SR5b/LI5b SR7a/LI7a SR7b/LI7b	I / I/O	I	**S/T Receive Channel 1, 3, 5, 7 / U_{PN} Transmit/Receive Channel 1, 3, 5, 7**
12 13 28 27 48 47 73 74	LI0a LI0b LI2a LI2b LI4a LI4b LI6a LI6b	I/O	I	**U_{PN} Transmit/Receive Channel 0, 2, 4, 6**
21 22 35 36 66 65 80 79	SX1a SX1b SX3a SX3b SX5a SX5b SX7a SX7b	O	O	**S/T Transmit Channel 1, 3, 5, 7**
8, 9, 31, 32, 51, 52, 69, 70	n.c.	-	-	**n**ot **c**onnected

Table 3 PEB 20591: U_{PN} and S/T Line Interface

Pin No.	Symbol	In (I) Out(O)	During Reset	Function
12 13 25 26 27 28 39 40 48 47 62 61 73 74 76 75	SR0a/LI0a SR0b/LI0b SR1a/LI1a SR1b/LI1b SR2a/LI2a SR2b/LI2b SR3a/LI3a SR3b/LI3b SR4a/LI4a SR4b/LI4b SR5a/LI5a SR5b/LI5b SR6a/LI6a SR6b/LI6b SR7a/LI7a SR7b/LI7b	I / I/O	I	**S/T Receive Channel / U_{PN} Transmit/Receive Channel**
8 9 21 22 32 31 35 36 52 51 66 65 69 70 80 79	SX0a SX0b SX1a SX1b SX2a SX2b SX3a SX3b SX4a SX4b SX5a SX5b SX6a SX6b SX7a SX7b	O	O	**S/T Transmit Channel**

Table 4 IOM-2000 Interface

Pin No.	Symbol	In (I) Out (O)	During Reset	Function
18	FSC	I	I	IOM-2000 **F**rame **S**yn**C**hronization 8 kHz signal for IOM-2000 frames
19	DCL_2000	I	I	IOM-2000 **D**ata **CL**ock Data Clock from DELIC (3.072, 6.144 or 12.288 MHz in case of 1, 2 or 3 VIPs)
1	DR	O	O	IOM-2000 **D**ata **R**eceive Data received on the line interface is sent to the DELIC
20	DX	I	I	IOM-2000 Data Transmit Data to be transmitted on the line interface is received from the DELIC.
2	CMD	I	I	IOM-2000 **C**om**M**an**D** Receives the commands from the DELIC.
3	STAT	O	O	IOM-2000 **STAT**us Transmits the VIP status information to the DELIC.
4	REFCLK	O	O	IOM-2000 **REF**erence **CL**oc**K** Provides a 1.536 MHz reference clock (e.g. derived from Central Office in LT-T applications) to the DELIC

Table 5 Clock Signals and Dedicated Pins

Pin No.	Symbol	In (I) Out (O)	During Reset	Function
42 43	CLK15-I CLK15-O	I O	I O	15.36-MHz External Crystal Input 15.36-MHz External Crystal Output
17	INCLK	I	I	External Reference **CL**oc**K IN**put Reference clock from VIP or Central Office
33 34	VIP_ADD0 VIP_ADD1	I	I	**VIP ADD**ress Pins Determines the sequential order of up to 3 VIPs in the IOM-2000 frame for the 12-MHz case: VIP_ADD(1:0) '00' = VIP in 1st quarter of IOM-2000 frame '01' = VIP in 2nd quarter of IOM-2000 frame '10' = VIP in 3rd quarter of IOM-2000 frame '11' = Reserved for future connection of VIP in 4th quarter of IOM-2000 frame. Currently only the lower addresses are available. (refer to IOM-2000 description in DELIC-LC/ -PB Data Sheet)
16	IDDQ	I	I	**IDDQ** Test Mode Forces the Line Interface Unit into power down mode for IDDQ testing.
41	POWDN	I	I	Oscillator **POW**er **D**ow**N** Switches the internal oscillator into power down mode (in case that 15.36-MHz input clock is provided by the DELIC)
5	DIR	O	O	**DIR**ection of Transfer on U_{PN} Line Interface Indicates the direction of the data transfer (Tx or Rx) in U_{PN} ping-pong mode (required for driving electronic transformers).
60	SCANEN	I	I	**SCAN EN**able If driven to '1' during device tests, a full scan of the VIP is enabled.

Table 6 Power Supply and Reset

Pin No.	Symbol	In (I) Out (O)	During Reset	Function
11, 24, 29, 38, 49, 63, 67, 72, 77	V_{DDA}	I	I	Power Supply 3.3 V Analog Used for VIP analog logic
6, 14, 45, 53	V_{DDD}	I	I	Power Supply 3.3 V Digital Used for VIP digital logic
10, 23, 30, 37, 50, 64, 68, 71, 78	V_{SSA}	I	I	Reference Ground (0 V) Analog
7, 15, 46, 54	V_{SSD}	I	I	Reference Ground (0 V) Digital
44	$\overline{\text{RESET}}$	I	'low'	System Reset VIP is forced to go into reset state.

Table 7 JTAG Boundary Scan Test Interface (IEEE 1149.1)

Pin No.	Symbol	In (I) Out (O)	During Reset	Function
58	TCK	I	I	**T**est **C**loc**K** Provides a clock for JTAG test logic.
57	TMS	I	I	**T**est **M**ode **S**elect (internal pull-up) A '0' to '1' transition on this pin is required to step through the TAP controller state machine.
56	TDI	I	I	**T**est **D**ata **I**nput (internal pull-up) In the appropriate TAP controller state, test data or a instruction is shifted in via this line.
59	TDO	O	O	**T**est **D**ata **O**utput In the appropriate TAP controller state, test data or a instruction is shifted out via this line.
55	$\overline{\text{TRST}}$	I	I	**T**est **R**e**S**e**T** (internal pull-up) Provides an asynchronous reset to the TAP controller state machine.

3 Interface Description

The VIP provides four types of external interfaces: U_{PN} line interfaces, S/T line interfaces, an IOM-2000 interface and a JTAG boundary scan test interface. These interfaces are described in the following sections:

3.1 Overview of Interfaces

The VIP provides the following system interfaces:

- **U_{PN} line interfaces**
  The VIP provides up to 8 independent U_{PN} line interfaces for connection of ISDN terminals or DECT base stations.
- **S/T line interfaces**
  The PEB 20590 provides up to 4 independent S/T line interfaces (up to 8 for PEB 20591). They can be operated in subscriber mode (LT-S) or trunk mode (LT-T).
- **IOM-2000 interface**
  – Up to three VIPs can be connected to one DELIC via the IOM-2000 interface.
  – VIP's transceivers are initialized and controlled by the DELIC.
- **JTAG boundary scan test interface**
  – The VIP provides a standard test interface according to IEEE 1149.1.
  – User-specific instructions are implemented to generate periodic test patterns on the line.
  – The TAP controller has an own reset input.

3.2 U_{PN} Line Interface

The functionality is compatible to OCTAT-P (PEB 2096). 1:1 transformers are required.

3.2.1 Frame Structure

The U_{PN} interface uses a ping-pong technique for 2B+D data transmission over the line. U_{PN} is always point-to-point.

The frame structure of the data transfer between the exchange (PBX, LT) and the terminal (TE) is depicted in **Figure 9**.

- The PBX starts a transmission every 250 µs (burst repetition period).
- A frame transmitted by the exchange (PBX) is received by the terminal (TE) after a given propagation delay t_d.
- The terminal waits a minimum guard time (t_g = 5.2 µs) while the line clears. Then a frame is transmitted from the terminal to the PBX.

- The time between the end of reception of a frame from the TE and the beginning of transmission of the next frame by the LT must be greater than the minimum guard time. The guard time in TE is always defined with respect to the M-bit.

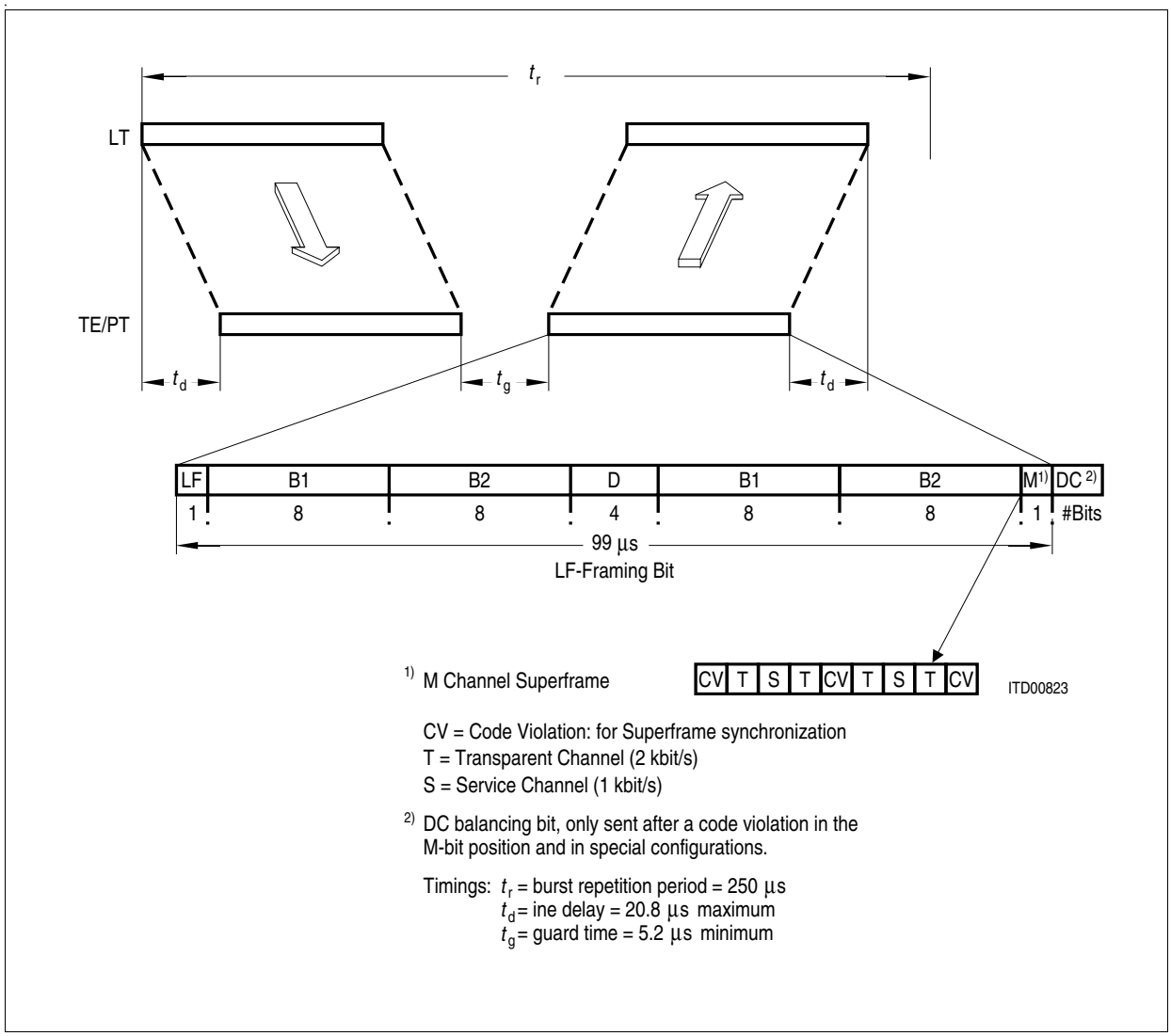


Figure 9 U_{PN} Interface Frame Structure

Data Rates

Within a burst, the U_{PN} data rate is 384 kbit/s using a 38-bit frame structure. During the 250-µs burst repetition period, 4 D-bits, 16 B1-bits and 16 B2-bits are transferred in each direction, resulting in a full-duplex user data rate of 144 kbit/s.

Control and Maintenance Bits

Bit	Description
LF	Framing Bit Always logical ‘1’.
M	M-Bit Final bit of the frame. Four successive M-bits compose a superframe. Three signals are carried in this superframe:
CV	Code Violation Bit First bit of the superframe. Used for superframe synchronization.
S	Service Bit Third bit of the superframe. Accessible via DELIC’s command/status interface. Conveys test loop control information from the PBX to the TE and reports transmission errors from the TE to the PBX (far-end code violation).
T	T-Bit 2nd and 4th bit of the superframe. Accessible via DELIC’s command/status interface. Carries the D-channel "available/blocked" information for the terminal and the DECT synchronization information.
DC	DC Balancing Bit May be added to the burst to decrease DC offset voltage on the line after transmission of a CV in the M-bit position. VIP issues this DC balancing bit when transmitting INFO 4 (line activated and synchronized), and when line characteristics indicate a potential decrease in performance. DELIC is able to enable or disable this feature (via the DELIC BBC command bit).

U_{PN} Coding

The coding technique used in the VIP transceiver is half-bauded AMI code with a 50 % pulse width (refer to **Figure 10**).

Binary Value	AMI Code with 50 % Pulse Width
Logical ‘0’	Neutral level
Logical ‘1’	Alternate positive and negative pulses

A Code Violation (CV) is caused by two successive pulses with the same polarity.

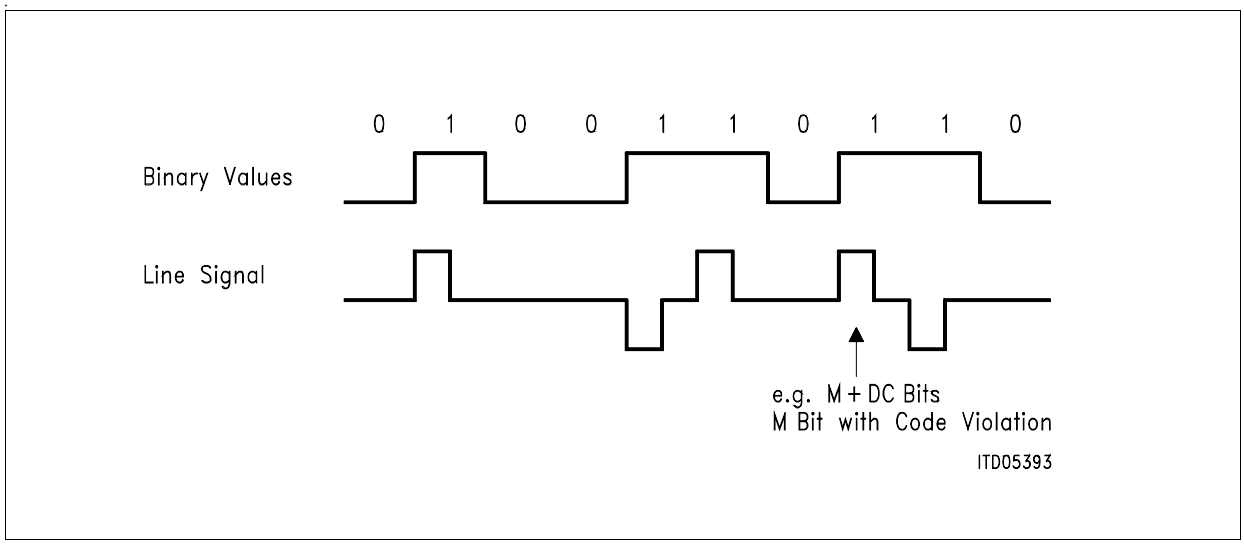


Figure 10 AMI Coding on the U_{PN} Interface in VIP

Scrambling / Descrambling

B-channel data on the U_{PN} interface is scrambled to ensure that the receiver at the subscriber terminal gets enough pulses for a reliable clock extraction (flat continuous power density spectrum), and to avoid periodical patterns on the line. The scrambler/ descrambler polynomial implemented in DELIC complies with ITU-T V.27 and OCTAT-P.

3.2.2 U_{PN} Transceiver

The receiver input stages consist of an amplifier/equalizer, followed by a peak detector adaptively controlling the thresholds of the comparators and a digital oversampling unit.

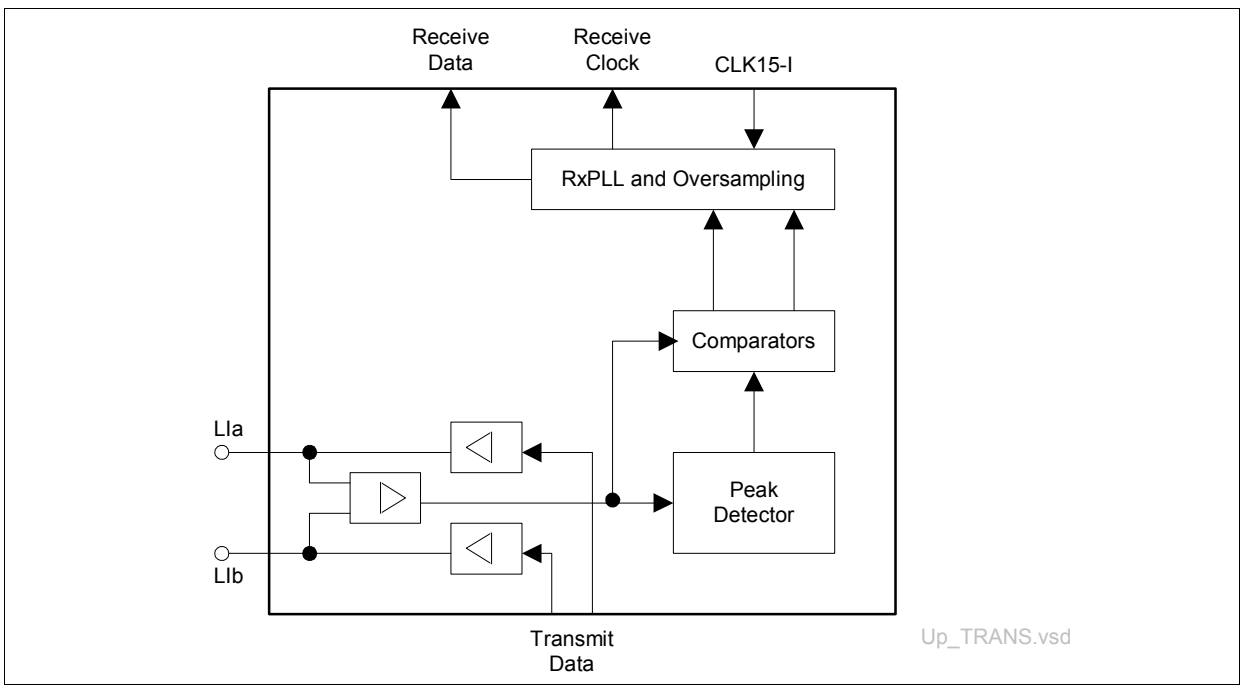


Figure 11 Transceiver Functional Blocks

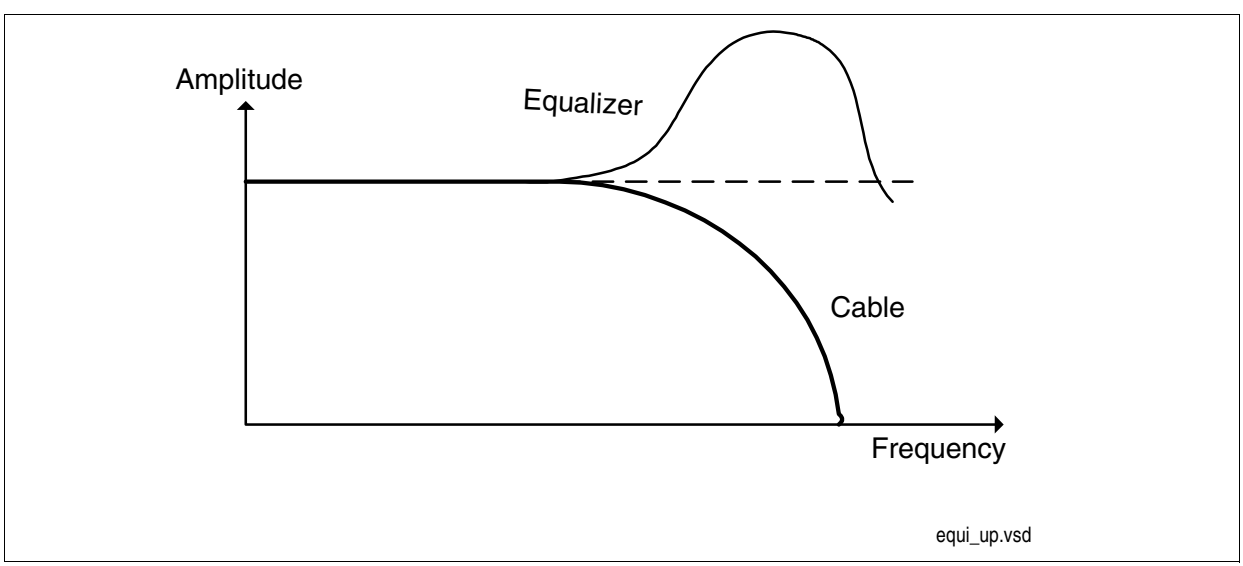


Figure 12 Equalizer Effect

The equalizer compensates the loss of Amplitude of higher frequencies (see **Figure 12**). In order to reach the best performance and range of the U_{PN} transceiver, it is recommended to use the equalizer with automatic adaptation.

To enable the filter of equalizer inside the VIP, set bit TICCMR:FIL to ’1’ (please refer to VIP channel config description in DELIC-LC/-PB SW User’s Manual). The adaptive amplifier control of the equalizer should be set to automatic. Set bit TICCMR:AAC (1:0) to ’00’ (please refer to VIP channel config description in DELIC-LC/-PB SW User’s Manual).

3.2.3 Receive PLL

The receive PLL (RxPLL) recovers bit timing from a comparator output signal.

Note: The recommended setting for the receive PLL is integral behaviour. This is enabled by setting bit TICCMR:PLLINT=’1’ (please refer to VIP channel config description in DELIC-LC/-PB SW User’s Manual).

Comparator threshold.

The comparator has a threshold of 80 % with respect to the signal stored by the peak detector.

Phase adjustment.

The RxPLL performs tracking after detecting phase shifts of the same polarity in four consecutive pulses. A phase adjustment is done by adding or subtracting 65 ns or 32.5 ns (one U_{PN} oscillator period), programmable by the DELIC command bit ’PLLS’ (default TICCMR:PLLS ’0’), to or from the 384 kHz receive data clock.

3.2.4 Receive Signal Oversampling

In order to further reduce the bit error rate in severe conditions, the VIP performs oversampling of the received signal and uses majority decision logic. The process of receive signal oversampling is illustrated in **Figure 13**:

- Each received bit is sampled 6 times at 15.36-MHz clock intervals inside the estimated bit window.
- The samples obtained are compared to a threshold of 50 % with respect to the signal stored by the peak detector.
  If at least ’n’ samples have an amplitude exceeding the 50 % threshold, a logical ’1’ is detected; otherwise a logical ’0’ (no signal) is assumed.
  The parameter ’n’ is programmed in steps of 2 in bits OWIN(2:0) of IOM-2000 CMD register.

Note: The recommended setting for signal oversampling is TICCMR:OWIN =’011’. For detailed description please refer to DELIC-LC/-PB Data Sheet.

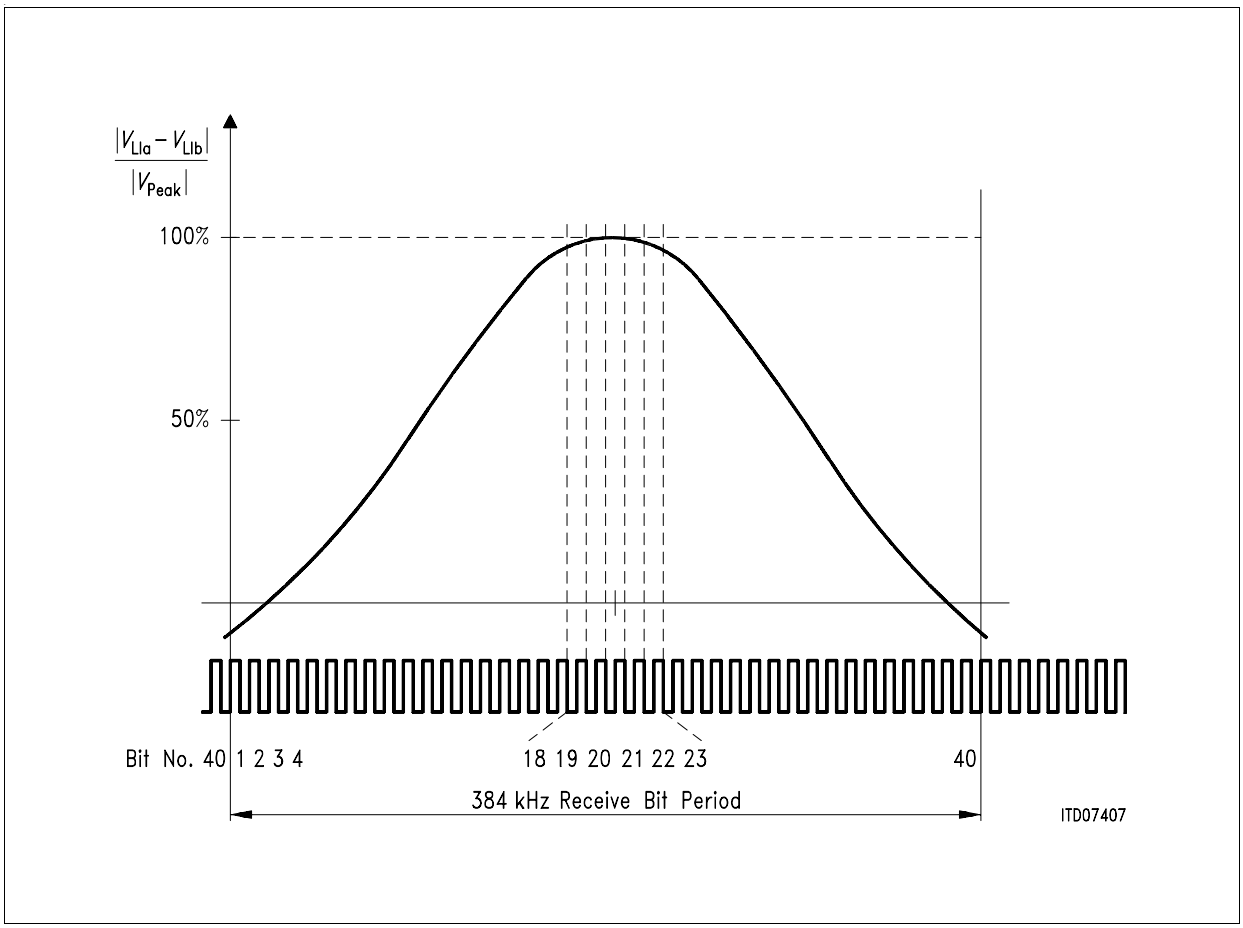


Figure 13 Receive Signal Oversampling on U_{PN} Interface

3.3 S/T Line Interface

The functionality is compatible with that of QUAT-S (PEB 2084). External protection circuitry is reduced, and 1:1 transformers are required.

3.3.1 Frame Structure

The S/T interface uses two pairs of copper wires (dedicated to transmit and receive) for 2B+D data transfer. It builds a direct link between the VIP and connected subscriber terminals or the Central Office. It supports point-to-point or point-to-multipoint modes.

Data and maintenance information is accessible by DELIC via the IOM-2000 interface.

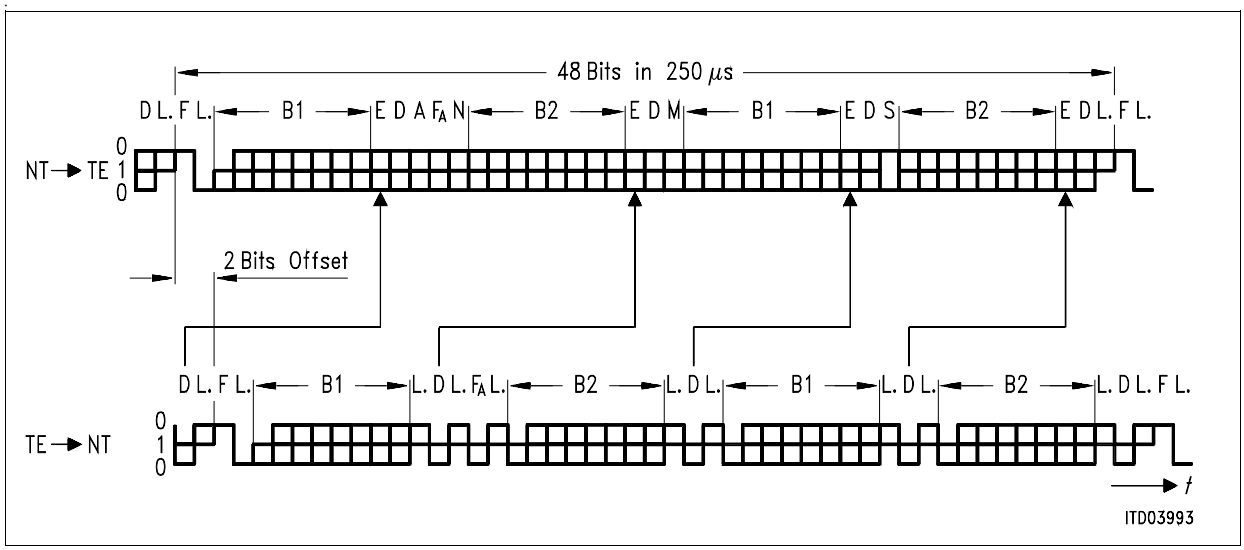


Figure 14 Frame Structure at Reference Points S and T (ITU-T I.430)

Bit	Description
F	Framing Bit F = (0b) → code violation, identifies a new frame (always positive pulse)
L.	DC Balancing Bit L. = (0b) → number of binary ZEROs sent after the previous L. bit was odd
D	D-Channel Data Signaling data specified by user
E	D-Channel Echo Bit E = D if D-channel is not blocked, otherwise E = $\overline{D}$. (ZEROs always overwrite ONEs)
F_A	Auxiliary Framing Bit See section 6.3 in ITU I.430
N	N = $\overline{F_A}$
B1	B1-Channel Data User data
B2	B2-Channel Data User data

Bit	Description
A	Activation Bit A = (0b) → INFO 2 transmitted A = (1b) → INFO 4 transmitted
S	S-Channel Data Bit S1 and S2 channel data
M	Multiframing Bit M = (1b) → Start of new multi-frame

Data Rates

The S/T transmission rate is 192 kbit/s (36 bits user data and 12 bits control and maintenance). Frames are transmitted with a 2-bit offset in TE/LT-T → LT-S direction.

S/T Coding

The coding technique used on the S/T interface is a full-bauded AMI code with 100 % pulse width (refer to **Figure 15**).

Binary Value	AMI Code with 100 % Pulse Width
Logical ‘0’	Alternate positive and negative pulses. There are two exceptions: • The first binary ’0’ following the first DC balancing bit is of the same polarity as the DC bit, • The F-bit is always at positive level (required code violations).
Logical ‘1’	No line signal (0 V)

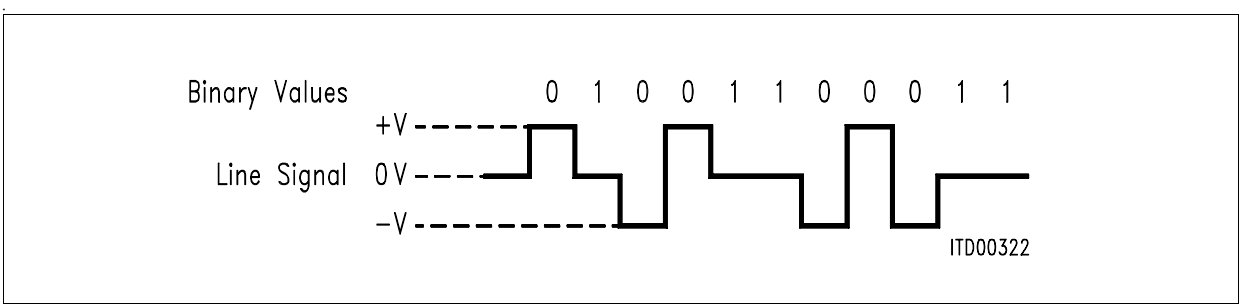


Figure 15 S/T Interface Line Code (without Code Violation)

3.3.2 S/T Transceiver

Receiver Characteristics

The receiver input stages consist of a differential amplifier, followed by a peak detector and a set of comparators. Additional noise immunity is achieved by digital oversampling after the comparators, meaning that the sampling of the received bit is controlled digitally and dependent on the mode (Command Register).

The peak detector requires at most 2 µs to reach the peak value while storing the peak level for at least 250 µs. The data detection thresholds are set to 35 % of the peak voltage to increase the performance in extended passive bus configurations. However, they are never lower than 85 mV with respect to the line signal level in order to increase noise immunity.

The level detector monitors the line input signals to detect whether an INFO signal is present. It is possible to indicate an incoming signal during activated analog loop.

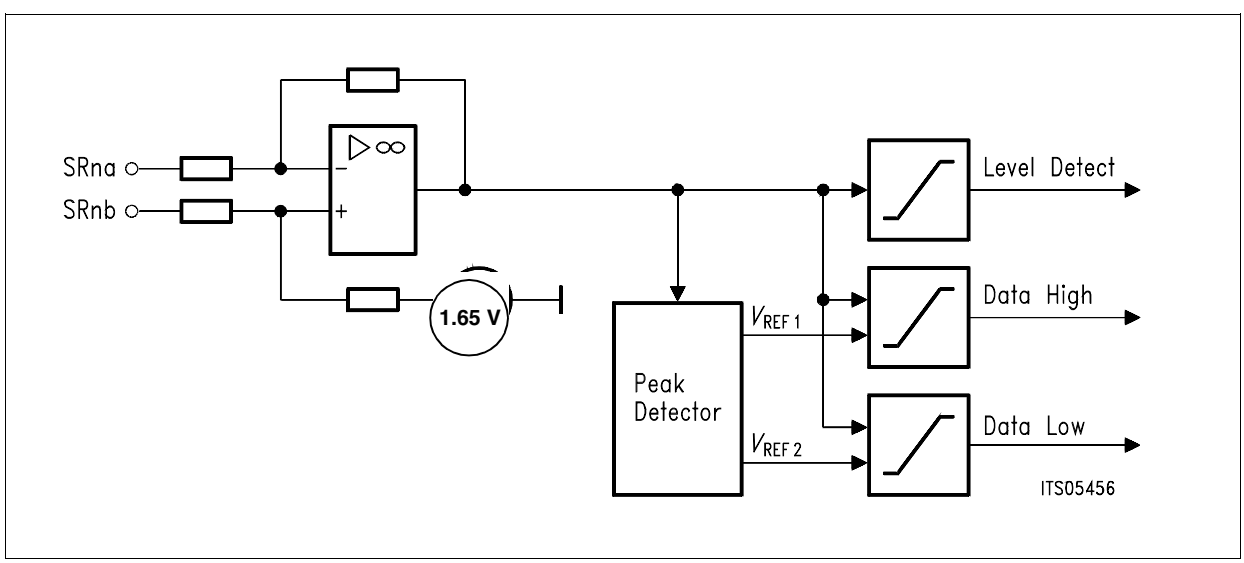


Figure 16 Receiver Functional Blocks

3.3.3 Receive Clock Recovery

The VIP generates the internal clocks with a PLL, that receives a 15.36-MHz signal via an on-chip oscillator either from an external crystal or from the DELIC.

VIP Operating Mode	All Clocks Synchronized to
LT-S or U_{PN} mode	IOM-2000 interface data clock provided by the DELIC on DCL_2000 pin
LT-T mode	Data clock provided by the Central Office

3.3.3.1 LT-S Mode

In the LT-S mode, the DELIC is the clock master to all terminals connected to the VIP. In receive direction, two cases are distinguished, depending on the bus configuration:

- Point-to-point or extended passive bus
- Short passive bus.

Point-to-Point or Extended Passive Bus

- Programmed by DELIC IOM-2000 Command bits:
  MOSEL(1:0) = ’00’ MODE(2:0) = ’011’
- The 192-kHz receive bit clock is recovered (via PLL) from the receive data stream on the S interface.
- Shift between receive and transmit frame:
  According to ITU-T I.430, the receive frame may be shifted by 2 to 8 bits with respect to the transmit frame. VIP supports also other frame shifts, including 0.

Note: The recommended setting for point-to-point and extended passive bus in LT-S mode is TICCMR:OWIN=’101’ and TICCMR:PD=’0’. For detailed description please refer to VIP channel config command in the DELIC-LC/-PB SW User’s Manual.

Short Passive Bus

- Programmed by DELIC IOM-2000 Command bits:
  MOSEL(1:0) = ’00’, MODE(2:0) = ’111’
- The 192-kHz receive bit clock is identical to the transmit bit clock generated by division of the incoming IOM-2000 data clock.
- Shift between receive and transmit frame:
  The sampling instant for the receive bits is shifted by 4.6 µs with respect to the transmit bit clock. According to ITU-T I.430, the receive frame must be shifted (delayed) by two bits with respect to the transmit frame.

Note: If one VIP has channels working in LT-S and U_{PN} mode, then the F-bits appear on the S interface 6 U_{PN} clocks (nominal case) later than the F-bits on the U_{PN} lines (within the same sync frame).

Note: The recommended setting for short passive bus in LT-S mode is TICCMR:OWIN=’001’ and TICCMR:PD=’0’. For detailed description please refer to VIP channel config command in the DELIC-LC/-PB SW User’s Manual.

3.3.3.2 LT-T Mode

- Programmed by DELIC IOM-2000 Command bits:
  MOSEL (1:0) = ’00’, MODE(2:0) = ’001’
- In LT-T applications, the VIP/DELIC system operates as slave to the central office clock.
- The 192-kHz receive bit timing is recovered (via RxPLL) from the receive data stream on the trunk line interface that was selected as clock source.
- The RxPLL also provides a 1.536-MHz clock synchronous to the Central Office clock (adaptive timing recovery), which in LT-T applications is used to synchronize the DELIC clock generator via the IOM-2000 REFCLK line; refer to **Figure 17**.
  The RxPLL tracks every 250 µs after detecting the phase between the framing bit transition (F/L-bit in S/T frame) of the receive signal and the recovered clock. A phase adjustment is done by adding or subtracting 65 ns or 130 ns to or from the 15.36-MHz clock depending on ’PLLS’.
- If several VIP or several S/T lines are operated in LT-T mode, only one trunk line may be selected to deliver the reference clock. The selection of this trunk line is programmed by the DELIC via IOM-2000 Command bits REFSEL(2:0) and EXREF.

Note: In LT-T mode, the transmit clock is identical to the recovered receive clock.

Note: The recommended setting for short passive bus in LT-T mode is TICCMR:OWIN=’101’ and TICCMR:PD=’1’. For detailed description please refer to VIP channel config command in the DELIC-LC/-PB SW User’s Manual.

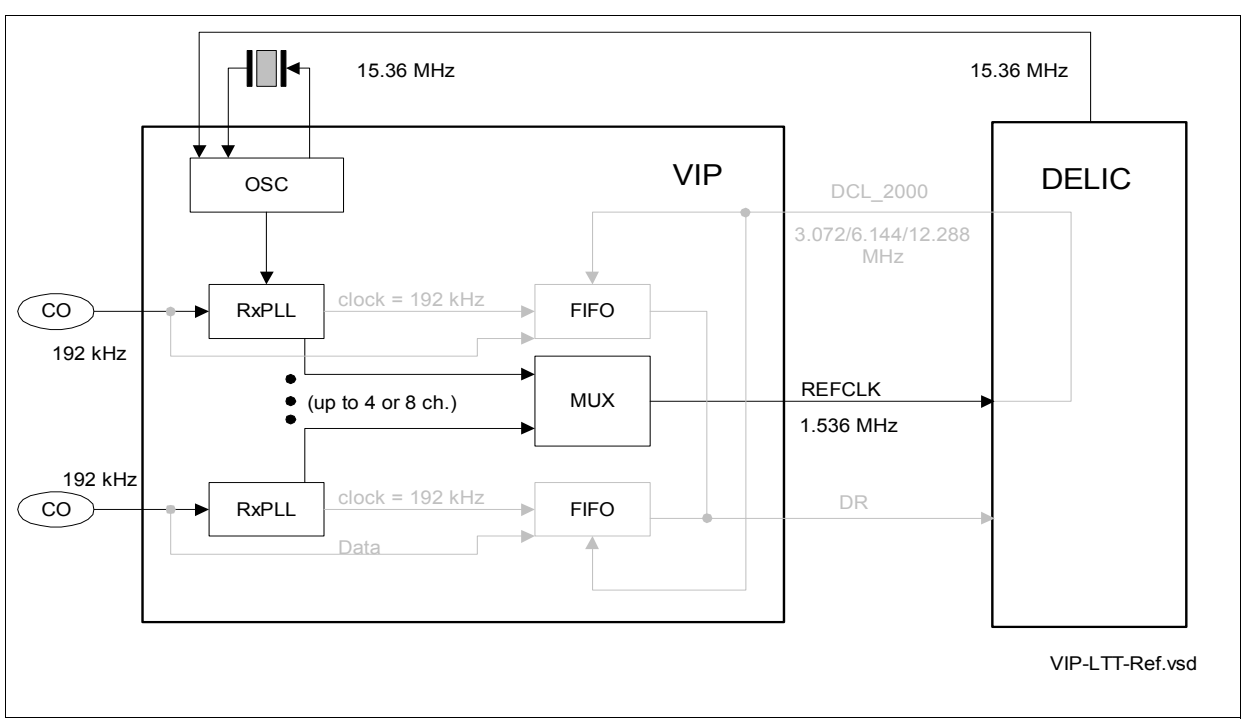


Figure 17 Clock Recovery in LT-T Mode

Jitter Requirements

In LT-T mode, ITU-T I.430 specifies a maximum jitter in transmit direction of – 7 % to + 7 %, resulting in 730 ns peak-to-peak.

This specification will be met by the VIP provided that the master clock source is accurate within 100 ppm.

3.3.4 Reference Clock Selection in LT-T Mode

In LT-T configurations, the DELIC receives the CO reference clock via the XCLK input pin, which is connected to VIP's REFCLK output.

The VIP reference clock channel is programmed by the DELIC. The source may be either one of the 8 VIP channels operated in LT-T mode or VIP's INCLK pin, when several VIP's are connected to the IOM-2000 interface (see **Figure 18**).

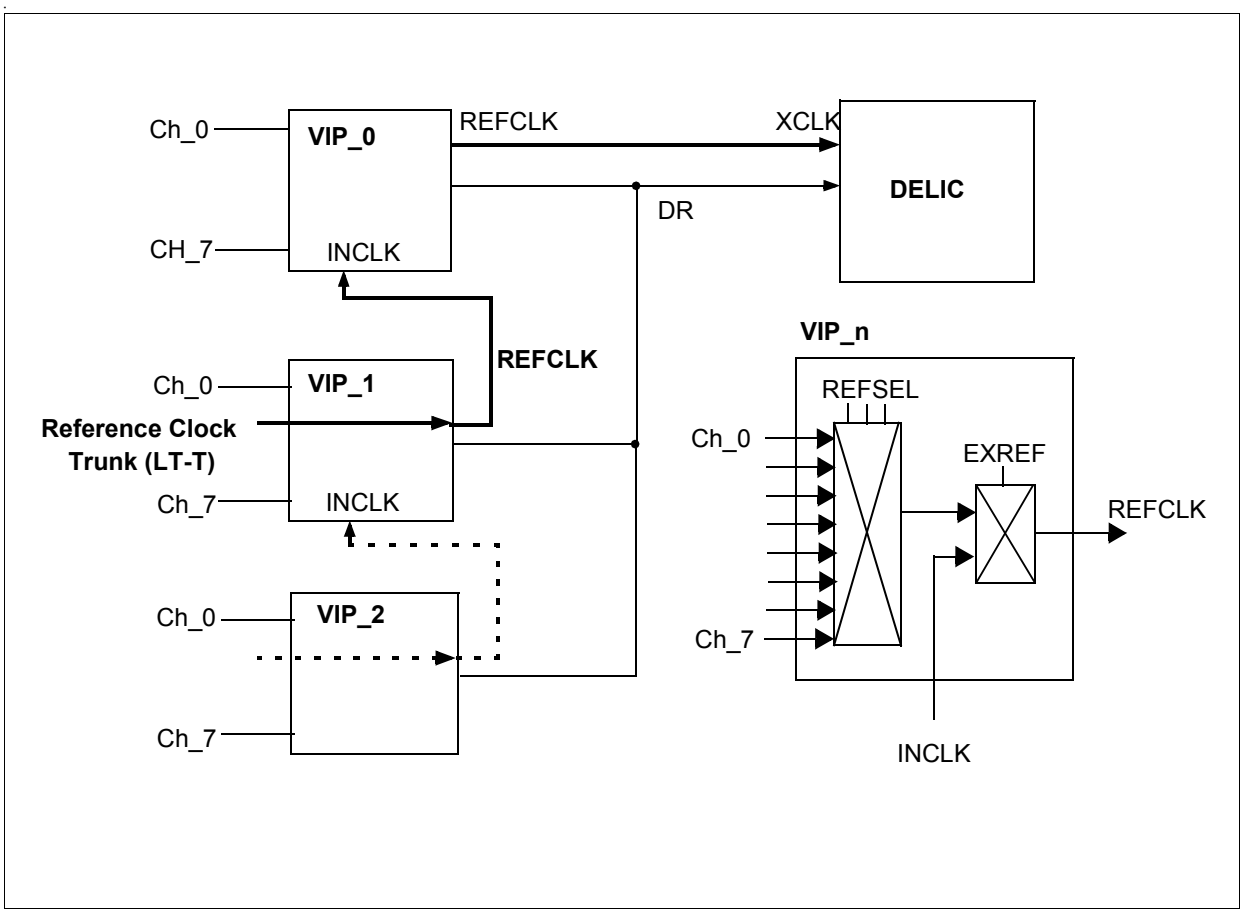


Figure 18 LT-T Reference Clock Channel Selection for Cascaded VIPs

3.3.5 Receive Signal Oversampling

The receive signal is oversampled within the receive clock period, and a majority logic is used to reduce the bit error rate in severe conditions.

- As illustrated in **Figure 19**, each received bit is sampled 29 times at 7.68-MHz clock intervals inside the estimated bit window.
- The samples obtained are compared against a threshold of 35% with respect to the signal stored by the peak detector.
  If at least a number of 'n' samples have an amplitude exceeding the threshold, a logical '0' is detected; otherwise a logical '1' (no signal) is assumed. The parameter 'n' is programmed by the OWIN command bits.

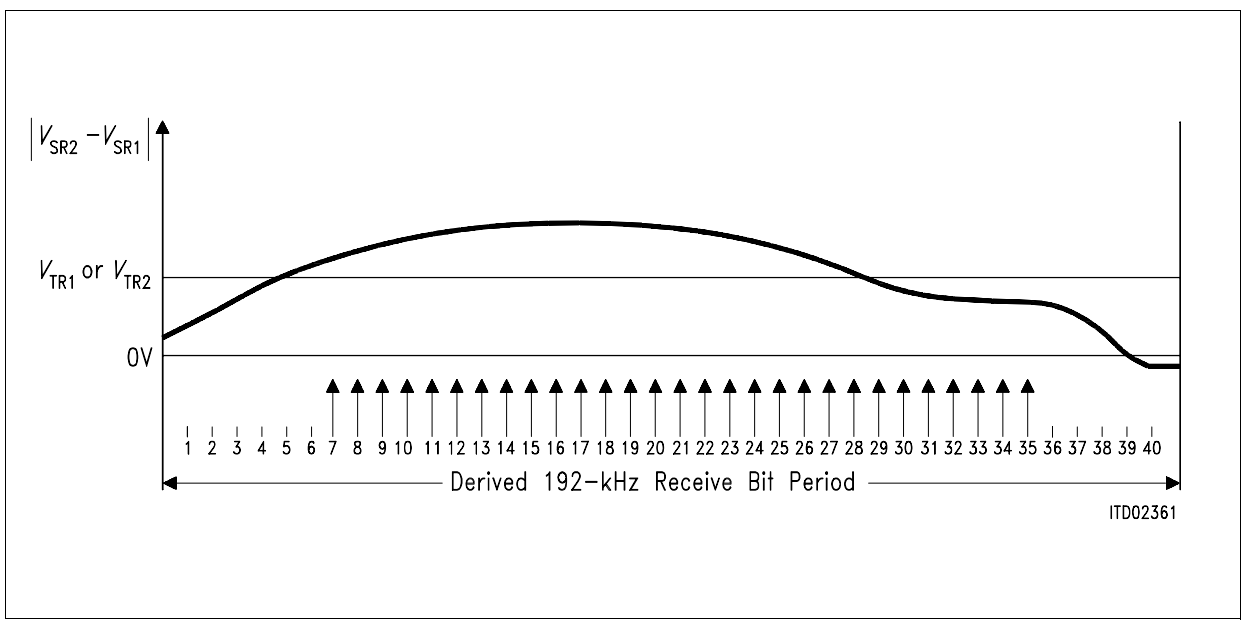


Figure 19 Receive Signal Oversampling in S/T Receiver

3.3.6 Elastic Buffer

A buffer in the VIP is designed as a wander-tolerant system, required in LT-T and LT-S modes. In LT-T mode, the VIP is clock slave to the CO, and the data clocks of the S/T interface and the IOM-2000 interface have a time dependent phase relationship. The buffer compensates a maximum phase wander of ± 20 µs.

A slip detector indicates when this limit is exceeded. The 'SLIP' bit in VIP Status Register issues a warning to the DELIC when a slip of 20 µs in either direction was detected. The VIP buffers are reset to their default positions automatically.

Note: In case of frame slip, the phase relationship between the IOM-2000 interface and the S/T interface is arbitrary. A re-alignment of the wander buffer after a slip may result in loss of data.

3.4 IOM-2000 Interface Overview

The IOM-2000 interface connects up to three VIPs to DELIC.

DELIC as the communication controller performs parts of the layer-1 protocol, which enables flexible and efficient operation of the VIP.

Note: For detailed description of IOM-2000, including the command and data interface, please refer to the DELIC Data Sheet.

IOM-2000	Description
Frame synchronization	IOM-2000 uses an 8-kHz FSC.
Data interface	Data is transmitted via DX line from DELIC to VIP with DCL_2000 rising edge. Data is received via DR line from VIP to DELIC, sampled with DCL_2000 falling edge.
Command/Status interface	Configuration and control information of VIP's layer-1 transceivers is exchanged via CMD and STAT lines.
Data/Command Clock	Data and commands for one VIP are transmitted at 3.072 MHz. When DELIC drives 2 or 3 VIPs, the transmission rate is increased.
Reference clock	In LT-T mode, the VIP provides a reference clock synchronized to the exchange. In LT-S or U_{PN} mode, DELIC is always the clock master to VIP.

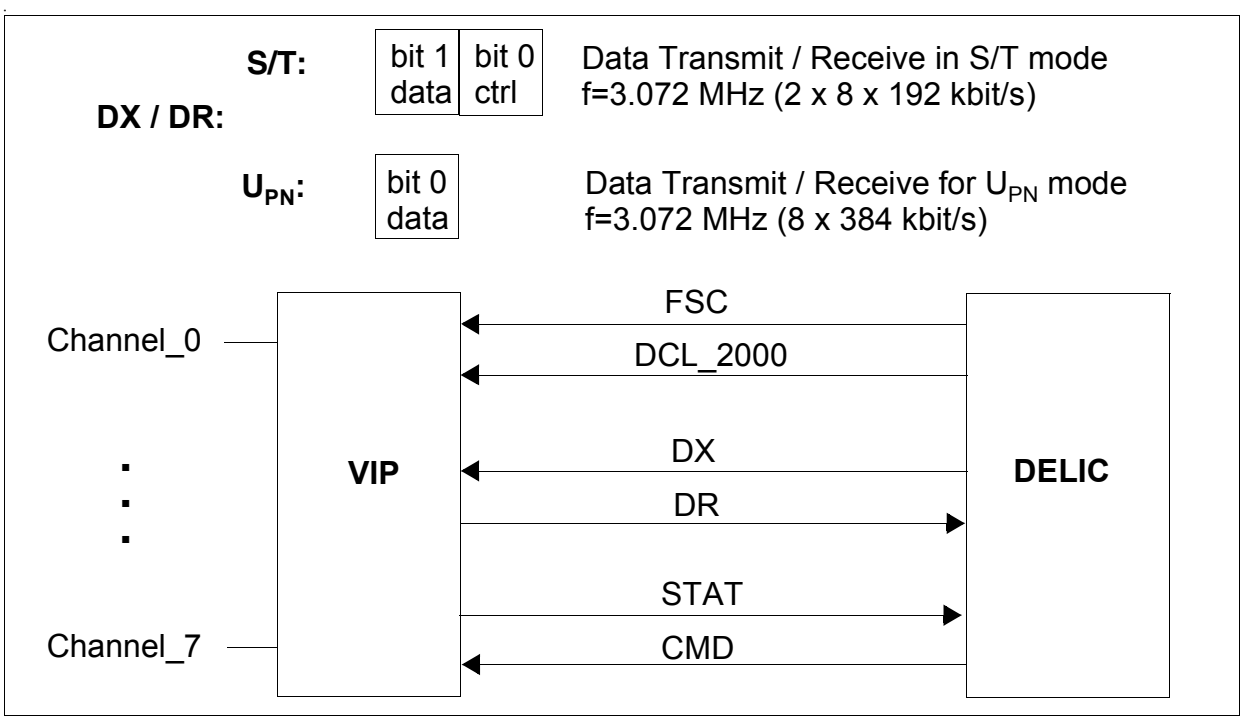


Figure 20 Overview of IOM-2000 Interface Structure (Example with One VIP)

3.4.1 IOM-2000 Frame Structure

3.4.1.1 Data Interface

On the ISDN line side of the VIP, data is ternary coded. Since the VIP contains logic to detect the level of the signal, only the data value is transferred via IOM-2000 to DELIC.

U_{PN} Mode

In U_{PN} mode, only data is sent via the IOM-2000 data interface.

S/T Mode

In S/T mode, data and control information is sent via IOM-2000 data interface. Every data bit has a control bit associated with it. Thus, for each S/T line signal, 2 bits are transferred via DX and DR. Bit0 is assigned to the user data, and bit1 carries control information.

Table 8 Control Bits in S/T Mode on DR Line

ctrl (bit1)	data (bit0)	Function
0	0	Logical ’0’ received on line interface
0	1	Logical ’1’ received on line interface
1	0	Received E-bit = inverted transmitted D-bit (E=$\overline{D}$) (LT-T only)
1	1	F-bit (Framing) received; indicates the start of the S frame

Table 9 Control Bits in S/T Mode on DX Line

ctrl (bit1)	data (bit0)	Function
0	0	Logical ’0’ transmitted on line interface
0	1	Logical ’1’ transmitted on line interface
1	0	not used
1	1	F-bit (Framing) transmitted; indicates the start of the S frame

*Note: ’data’ is always transmitted prior to ’ctrl’ via DX/DR lines (refer to **Figure 21**).*

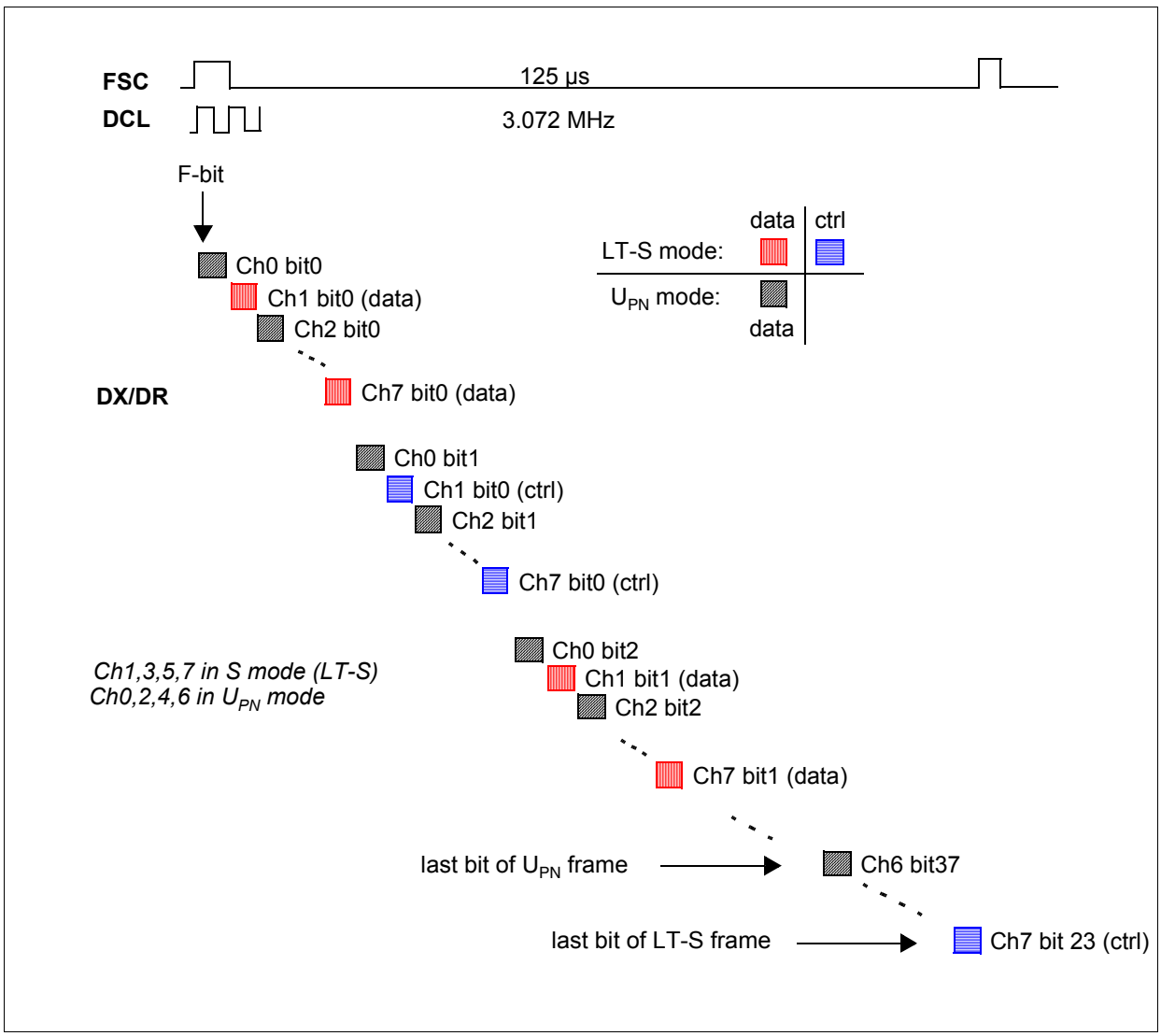


Figure 21 IOM-2000 Data Sequence (1 VIP with 8 Channels)

Note: 1. Data transfer on IOM-2000 interface always starts with the MSB (related to B channels), whereas CMD and STAT bits transfer always starts with LSB (bit 0) of any register

2. All registers follow the Intel structure (LSB=2^0, MSB=2^{31})

3. Unused bits are don't care ('x')

4. The order of reception or transmission of each VIP channel is always channel 0 to channel 7. A freely programmable channel assignment of multiple VIPs on IOM-2000 (e.g., ch0 of VIP_0, ch1 of VIP_0, ch0 of VIP_1, ch2 of VIP_0,...) is not possible.

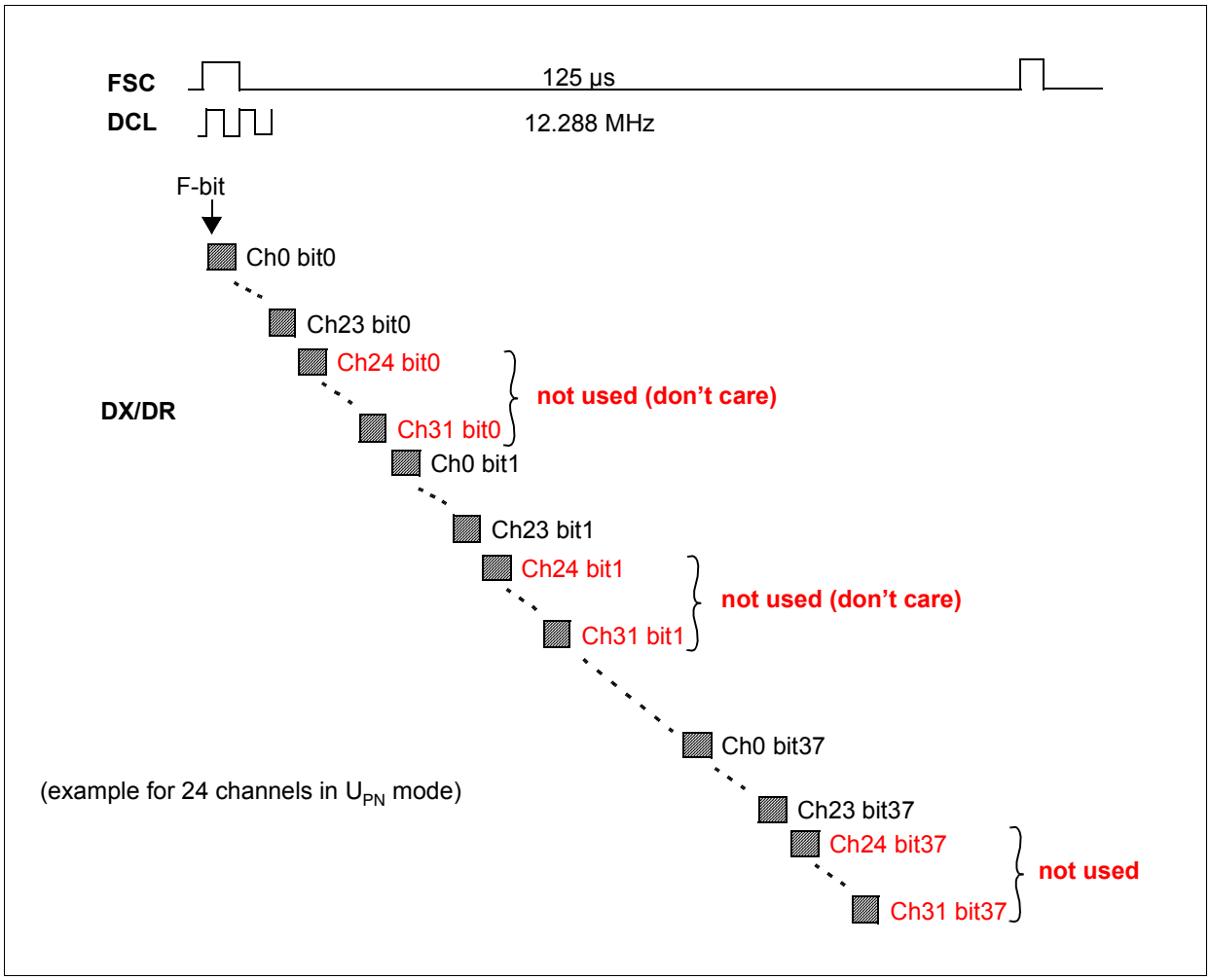


Figure 22 IOM-2000 Data Order (3 VIPs with 24 Channels)

Receive Data Channel Shift

In receive direction (DR), data of all IOM-2000 channels (ch0...7 if one VIP is used, ch0 ... ch23 if three VIPs are used) is shifted by 2 channels with respect to the transmitted data channels (DX), assuming a start of transmission of ch0 bit0 with the FSC signal. DELIC is transmitting ch0, while receiving ch2 via DR the same time, etc.

DX	ch0	ch1	ch2	ch3	ch4	ch5	ch6	ch7	ch0
DR	ch2	ch3	ch4	ch5	ch6	ch7	ch0	ch1	ch2

3.5 JTAG Boundary Scan Test Interface

The VIP provides IEEE 1149.1-compatible boundary scan support to allow cost-effective board testing. It consists of:

- Complete boundary scan test
- Test access port (TAP) controller
- Five dedicated pins: TCK, TMS, TDI, TDO (according to JTAG) and an additional $\overline{\text{TRST}}$ pin to enable asynchronous resets to the TAP controller
- One 32-bit IDCODE register
- Specific functions for the analog line interface pins LIna, b and SXna, b

3.5.1 TAP Controller

The TAP controller implements the state machine defined in the JTAG standard IEEE 1149.1. Transitions on the pin TMS cause the TAP controller to perform a state change.

The TAP controller supports 7 instructions:

- 5 standard instructions
- 2 additional user-specific instructions for transmitting continuous pulses at the line interfaces LIna/b (60 kHz) and SXna/b (120 kHz)

Table 10 TAP Controller Instruction Codes Overview

Code	Instruction	Function
0000	EXTEST	External testing
0001	INTEST	Internal testing
0010	SAMPLE/PRELOAD	Snap-shot testing
0011	IDCODE	Reading ID code register
1111	BYPASS	Bypass operation
1000	User specific	Continuous pulses on LIna and LInb
1001	User specific	Continuous pulses on SXna and SXnb

TAP Controller Instructions

EXTEST. EXTEST is used to verify the board interconnections.

When the TAP controller is in the state “update DR”, all output pins are updated with the falling edge of TCK. When it has entered state “capture DR” the levels of all input pins are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

INTEST . INTEST supports internal chip testing.

When the TAP controller is in the state “update DR”, all inputs are updated internally with the falling edge of TCK. When it has entered state “capture DR” the levels of all outputs are latched with the rising edge of TCK. The in/out shifting of the scan vectors is typically done using the instruction SAMPLE/PRELOAD.

Note: 0011 (IDCODE) is the default value of the instruction register.

SAMPLE/PRELOAD. SAMPLE/PRELOAD provides a snap-shot of the pin level during normal operation or is used to either preload (TDI) or shift out (TDO) the boundary scan test vector. Both activities are transparent to the system functionality.

Note: The input pin CLK15-I should not be evaluated.
The input frequency (15.36 MHz) is not synchronous with TCK (6.25 MHz); this may cause unpredictable snap-shots on the pin CLK15-I.

IDCODE. The 32-bit identification register is read out serially via TDO. It contains the version number (4 bits), the device code (16 bits) and the manufacturer code (11 bits). The LSB is fixed to ’1’.

The code for VIP version 2.1 is ’0010’.

Version	Device Code	Manufacturer Code		Output
0010	0000 0000 0100 1111	0000 1000 001	1	--> TDO

Note: In the state “test logic reset”, the code “0011” is loaded into the instruction code register.

BYPASS. A bit entering TDI is shifted to TDO after one TCK clock cycle, e.g. to skip testing of selected ICs on a printed circuit board.

User-Specific Instructions. Symmetric continuous pulses can be generated at pins LIna/b (60 kHz) and SXna/b (120 kHz) to test the analog line interfaces.

Note: A 15.36 MHz crystal or an external 15.36 MHz clock signal on CLK15-I is required for test pulse generation.

4 Operational Description

After some general remarks on the operation of the DELIC & VIP chipset, the reset and the initialization procedure are described. The operation of analog test loops as well as the monitoring of illegal code violations are also part of this chapter.

4.1 General

The DELIC & VIP chipset provides all functionality required for data transmission over the U_{PN} and the S/T interface, e.g., initialization and configuration, activation and deactivation, frame and multiframe synchronization.

The U_{PN} and S/T layer-1 state machines run on DELIC's DSP, performing activation/ deactivation, switching of loops and transmission of test pulse patterns. Such actions can be initiated by INFO signals on the U_{PN} and S/T lines, or by C/I codes sent by the µP to DELIC, and transferred to VIP via the IOM-2000 Command and Status interface. All options and register settings are described in the DELIC Data Sheet.

4.2 Reset

- At power-up, a reset pulse ($\overline{\text{RESET}}$ = low active) of at least 1 µs must be applied to reset the line interfaces of the VIP.
- The source of the reset can be either the microprocessor, or the DELIC $\overline{\text{RESIND}}$ pin, which is a delayed reset signal. This assures that the VIP is always reset simultaneously with the DELIC, and receives stable clock signals by the DELIC after reset.

4.3 Initialization

After hardware reset, each VIP must be initialized and configured by IOM-2000 commands. The following steps are required to initialize the VIP:

1. DELIC: Hardware Reset (to synchronize the state machines, counters etc.)
2. VIP: Hardware Reset
3. Release resets
4. Read version register from VIP-CMD register (optional) (available from VIP version V2.1 and higher)
5. Program the VIP if required, e.g. LT-T clock source
6. DELIC: Program VIP channel mode: U_{PN}, LT-S or LT-T, closing test loops
7. DELIC: Configure each VIP receiver if required, e.g. oversampling, D-channel handling.

4.4 Analog Test Loops

Different analog test loops may be switched in the VIP near to the S/T or U_{PN} line interfaces. No external U_{PN} or S/T interface circuitry is required to close these loops:

- Transparent analog loop, data forward path enabled
- Non-transparent analog loop, data forward path blocked
- External transparent analog loop, for board testing.

Initialization of Test Loops

Unlike the LT-T state machine, the LT-S and U_{PN} state machines in the DELIC do not support loops. Consequently neither the C/I commands nor indications are provided by the mailbox protocol. A loop can be programmed by setting bits TICCMR:LOOP and TICCMR:EXLP for the respective channel.

Note: For detailed description please refer also to the Application Note 'Test loops in the VIP'.

Transparency

In U_{PN} or LT-S mode, the user may output the loop-back data also transparently onto the line interface. The selection is performed via IOM-2000 TX_EN command. External analog loops are activated by EXLP Command bit (refer to **Chapter 6.3**).

Note: In order to guaranty that the loop is closed TX_EN must be set to one for the U_{PN} Interface

4.5 Monitoring of Code Violations

Any code violation on the S/T interface (according to ANSI T1.605), or code violations at positions other than the F-bit or M-bit in the U_{PN} frame result in VIP Status bit FECV being sent to DELIC. The check is performed once in every multiframe (every 20th 4-kHz S/T frame). To synchronize the checking, DELIC must issue the SH_FSC bit every 40th IOM frame.

5 Electrical Characteristics

This chapter contains the DC and AC specifications (as far as available) and timing diagrams.

5.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Storage temperature	T_{stg}	– 65 to 150	°C
IC supply voltage	V_{DD}	– 0.3 to 4.6	V
DC input voltage (except I/Os)	V_I	– 0.3 to 6.0	V
DC output voltage (including I/Os); output in high or low state	V_O	– 0.3 to V_{DD} + 0.3	V
DC output voltage (including I/Os); output in tri-state	$V_{I,}$ V_O	– 0.3 to 6.0	V
ESD robustness[1)] HBM: 1.5 kΩ, 100 pF	$V_{ESD,HBM}$	2000	V

1) According to MIL-Std 883D, method 3015.7 and ESD Ass. Standard EOS/ESD-5.1-1993. The SX pins are not protected against voltage stress > 1500 V (versus V_S or GND).

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

5.2 Operating Range

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Power supply voltage ±5%	V_{DD}	3.13	3.47	V
Ground	V_{SS}	0	0	V
Voltage applied to input pins	V_{IN}	0	$V_{DD} + 0.3$	V
Operating temperature	T_A	0	70	°C

Note: In the operating range the functions given in the circuit description are fulfilled.

5.3 DC Characteristics

V_{DD} = 3.3 V ± 0.17 V, T_A = 0 to 70°C

Table 11 DC Characteristics

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
All digital pins except LIna,b; SXna,b; SRna,b; CLK15-I,-O					
L-input voltage	V_{IL}		0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} + 0.3	V	
L-output voltage	V_{OL}		0.45	V	Iout = 2mA
H-output voltage	V_{OH}	2.4		V	Iout = 2 mA
Input leakage current	I_{LI}		± 1	µA	0 V ≤ V_{IN} ≤ V_{DD}; not specified for pins DIR and REFCLK.
TDI; TMS; $\overline{\text{TRST}}$					
Input leakage current high	I_{LIH}		1	µA	$V_{IN} = V_{DD}$
Input leakage current low	I_{LIL}	10	300	µA	V_{IN} = 0 V; internal pull-up resistor
LIna,b					
Transmitter output amplitude	V_X	2.24	3.08	V	U_{pn}-Transmitter output amplitude
Receiver input impedance	Z_R	10		kΩ	Receiver input impedance, transmitter inactive
SXna,b					
Absolute value of output pulse amplitude ($V_{SXna} - V_{SXnb}$)	V_X	1.05 1.05	1.16 1.23	V V	R_L = 50 Ω R_L = 400 Ω

Table 11 DC Characteristics (cont'd)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Transmitter output current	I_X		21.0 [1] 26.8 [2]	mA 	 R_L = 5.6 Ω
Transmitter output impedance	Z_X	acc. to ITU-T I.430 0		kΩ Ω	Inactive or during binary one, 0 V ≤ V_{IN} ≤ V_{DD} during binary zero

1) Nominal value determined by fuses
2) Absolute current limit resulting from the S interface specification

CLK15-I

H-input voltage	V_{IH}	1.2	V_{DD} + 0.3	V	
L-input voltage	V_{IL}		0.4	V	

CLK15-O

H-output voltage	V_{OH}	2.4		V	f = 0
L-output voltage	V_{OL}		0.45	V	f = 0

Supply Current

Operational supply current, Peak value	I_{CC}		30 + n × 27.5 + m × 47.5	mA	Peak supply current, V_{DD} = 3.3 V n = number of S/T interfaces activated m = number of U_{PN} interfaces activated
Operational supply current, Mean (typical) value	I_{CC}		18 + n × 8.5 + m × 6.5	mA	Mean supply current, V_{DD} = 3.3 V n = number of S/T interfaces activated m = number of U_{PN} interfaces activated

5.4 Capacitances

T_A = 25 °C; V_{DD} = 3.3 V ± 0.17 V, V_{SS} = 0 V, f_C = 1 MHz, unmeasured pins grounded

Table 12 I/O Capacitances (except line interfaces and clocks)

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Pin capacitance	$C_{I/O}$		7	pF	

5.5 Recommended 15.36-MHz Crystal Parameters

The user has two options to supply the VIP 15.36-MHz input clock:

- via a standard 15.36-MHz crystal or
- via an external source, e.g. connecting the DELIC output pin L1_CLK (duty cycle of 40:60 or better is required). The on-chip oscillator must be powered-down via pin POWDN.

Note: It is recommended to supply the VIP 15.36-MHz input clock via the DELIC.

In case a crystal (serial resonance) is connected, it should meet the requirements shown in **Table 13**.

Table 13 Recommended Crystal Parameters

Parameter	Symbol	Typical Values	Unit	Test Condition
Motional Capacitance	C_1	20	fF	
Shunt Capacitance	C_0	7	pF	
External Load Capacitance	C_L	≤ 30	pF	
Resonance Resistance	R_r	≤ 65	Ω	
Frequency Calibration Tolerance		≤ 100	ppm	

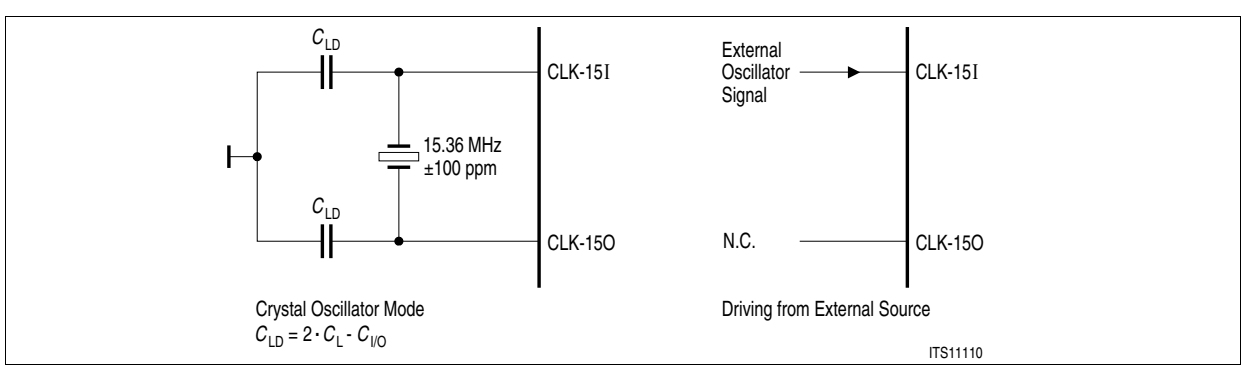


Figure 23 Recommended Oscillator Circuit

5.6 AC Characteristics

T_A = 0 to 70°C; V_{DD} = 3.3 V ± 0.17 V

Note: Timing measurements are made at 2.0 V for a logical '1' and at 0.8 V for a logical '0'.

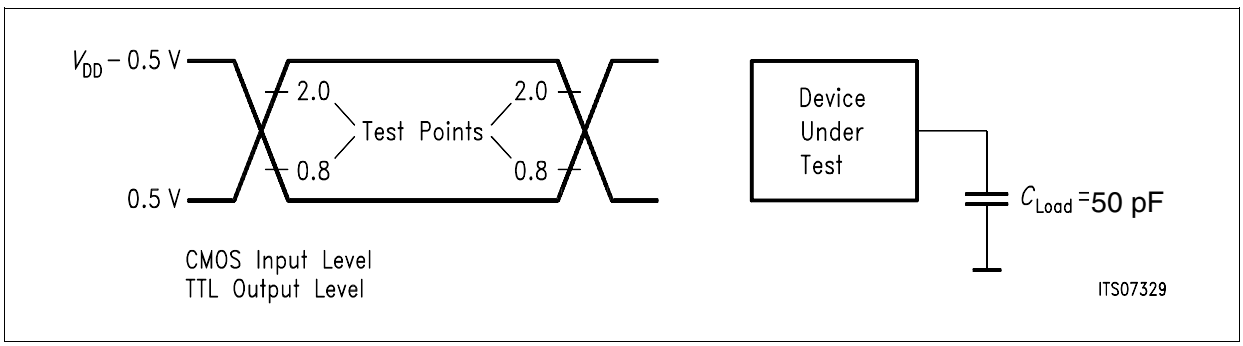


Figure 24 Input/Output Wave Form for AC Tests

5.7 REFCLK

.

Parameter	Symbol	Limit Values		Unit	Comment
		min.	max.		
High phase of clock	t_{WH}		40	ns	Delay of falling edge after falling edge of INCLK
Low phase of clock	t_{WL}		40	ns	Delay of rising edge after rising edge of INCLK
Clock period	T_P	651		ns	During PLL adjustment this value could change

5.8 U_{pn} Interface

Parameter	Symbol	Limit Values		Unit	Comment
		min.	max.		
DIR delay from DCL_2000 rising edge	t_{DIR}		60	ns	

5.9 IOM-2000 Interface

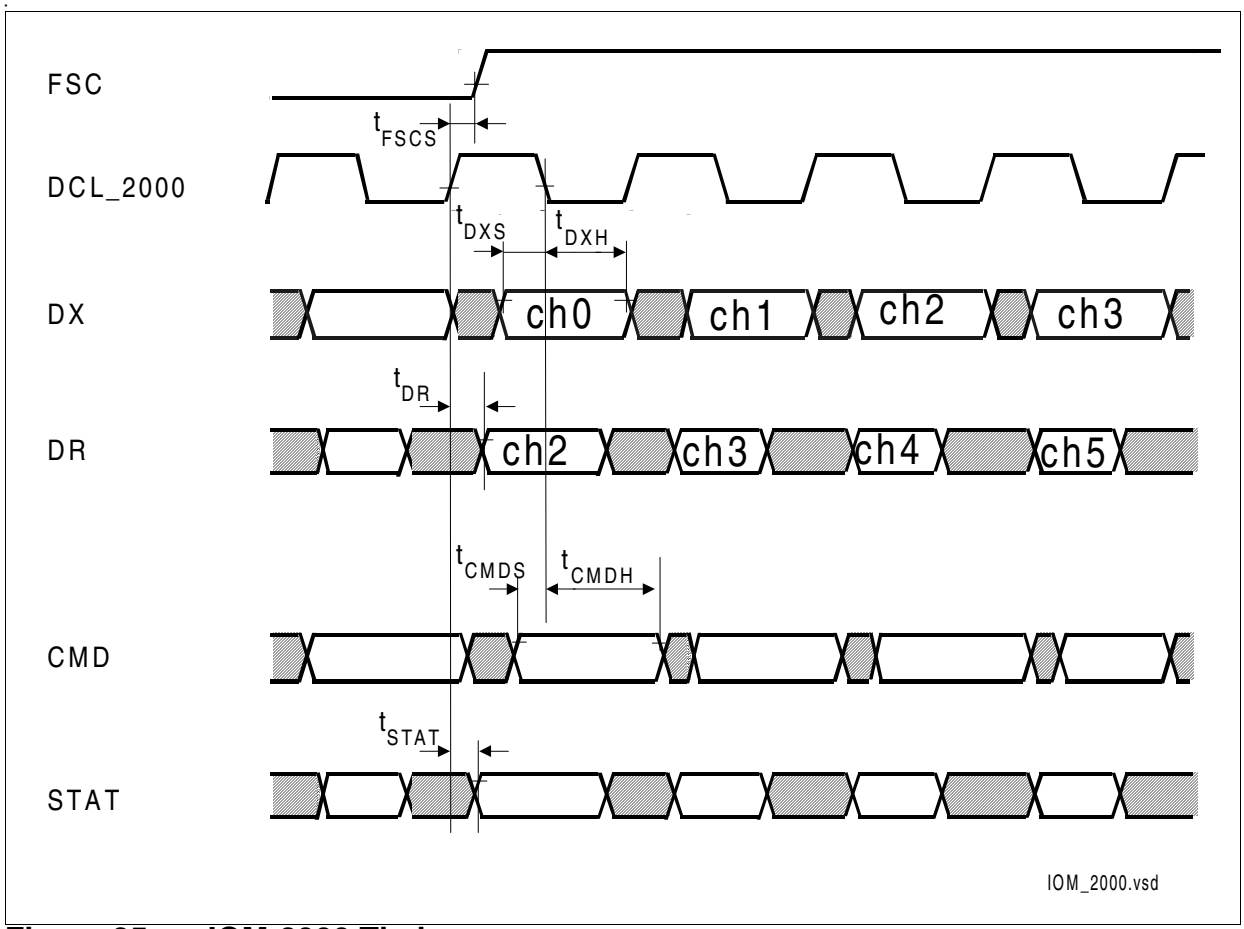


Figure 25 IOM-2000 Timing

Table 14 IOM-2000 Interface Timing

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
DR delay from DCL_2000 rising edge	t_{DR}			38	ns	
STAT delay from DCL_2000 rising edge	t_{STAT}			38	ns	
CMD setup time to DCL_2000 falling edge	t_{CMDS}	10			ns	
CMD hold time to DCL_2000 falling edge	t_{CMDH}	10			ns	

Table 14 IOM-2000 Interface Timing

Parameter	Symbol	Limit Values			Unit	Notes
		min.	typ.	max.		
FSC setup time before DCL_2000 rising edge	t_{FSCS}	-2		10	ns	
FSC hold time after DCL_2000 falling edge	t_{FSCH}	70			ns	not shown in **Figure 25**
DX setup time before DCL_2000 falling edge	t_{DXS}	10			ns	
DX hold time after DCL_2000 falling edge	t_{DXH}	10			ns	

5.10 JTAG Boundary Scan Test Interface

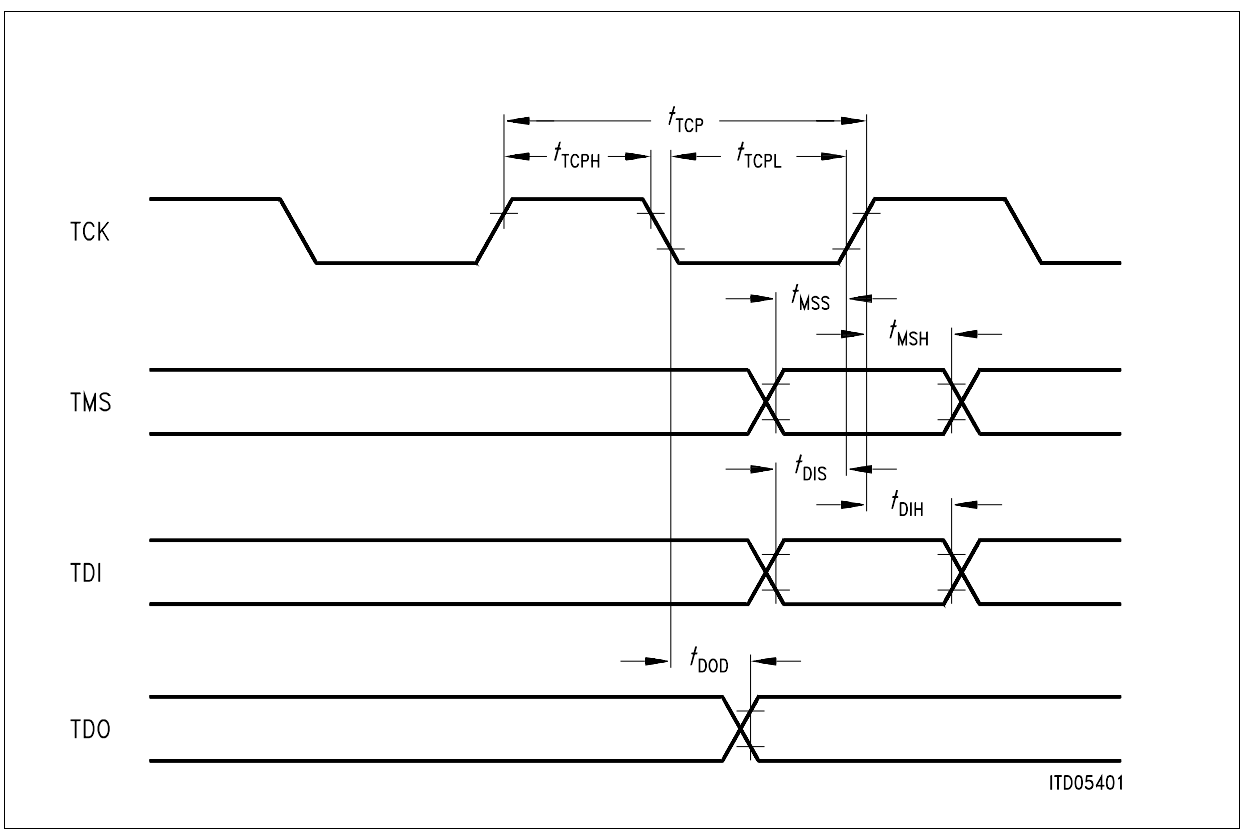


Figure 26 JTAG Timing

Table 15 JTAG Boundary Scan Timing Values

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Test clock period	t_{TCP}	100		ns
Test clock period low	t_{TCPL}	50		ns
Test clock period high	t_{TCPH}	50		ns
TMS setup time to TCK	t_{MSS}	10		ns
TMS hold time from TCK	t_{MSH}	10		ns
TDI setup time to TCK	t_{DIS}	10		ns
TDI hold time from TCK	t_{DIH}	10		ns
TDO valid delay from TCK	t_{DOD}		30	ns

5.11 U_{PN} Transmitter Performance

The VIP fulfills the electrical requirements of the U_{PN} interface for loop lengths, depending on the cable quality:

.

Adaptive Equalizer Switching is Enabled AAC(1:0) = '0x' and FIL = 1 in DELIC IOM-2000 Command Register	
Cable	**Loop Length**
J-Y (ST) Y 2 × 2 × 0.6	up to 1 km
AWG 26	up to 1.3 km

5.12 S/T Transmitter Performance

.

Cable 0.6 mm, 120 nF/km

Configuration	Condition	Distance TE-TE	Distance TE-LT
Point-to-point	no noise	–	1000
	200 / 2000 kHz 100 mVpp	–	950
Ext. passive bus	no noise	120m	750m
(Roundtrip < 2 µs)	200 / 2000 kHz 100 mVpp	120m	550m

6 Application Hints

This chapter provides some additional information on how to use the VIP. The first section describes some external circuitry: Recommended line transformers, resistors and capacitors. Different wiring configurations in user premises are depicted for the LT-S mode, and the different loops that can be closed in the VIP via the DELIC are also presented in the following sections.

6.1 VIP External Circuitry

6.1.1 Recommended Line Transformers

The VIP is connected to the U_{PN} or S/T lines via 1:1 transformers. The line side (primary side) of the transformer could be center-tapped for the phantom power supply.

Reference model parameters of the transformers are shown below.

U_{PN} Transformer

Primary to secondary transformer ratio:	1:1
Primary total DC resistance:	$R \leq 4..8\ \Omega$
Primary inductance:	$L_M > 2.1$ mH $\pm$ 20 %
Primary inductance with secondary short circuited:	$L_P < 22\ \mu$H
Coupling capacitance:	$C_K < 150$ pF

S/T Transformer

Primary to secondary transformer ratio:	1:1
Primary total DC resistance:	$R \leq 2\ \Omega$
Primary inductance:	$L_M > 30$ mH
Primary inductance with secondary short circuited:	$L_P < 6\ \mu$H
Coupling capacitance:	$C_K < 80$ pF

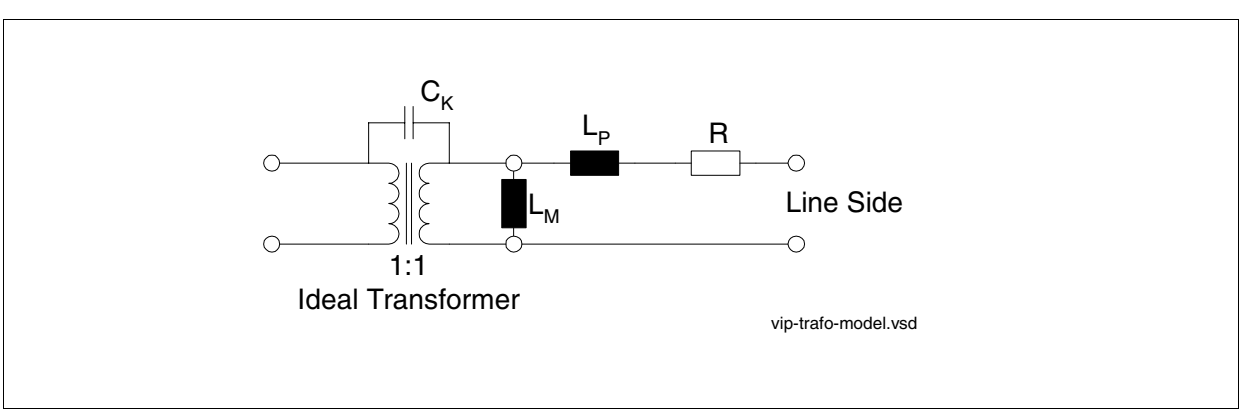


Figure 27 1:1 Transformer Model

6.1.2 U_{PN} Interface External Circuitry

A transformer, external resistors and two capacitors (100 nF and 0.33 µF) are connected externally to the line interface pins LIna,b. Voltage overload protection is achieved by adding clamping diodes (see **Figure 28**).

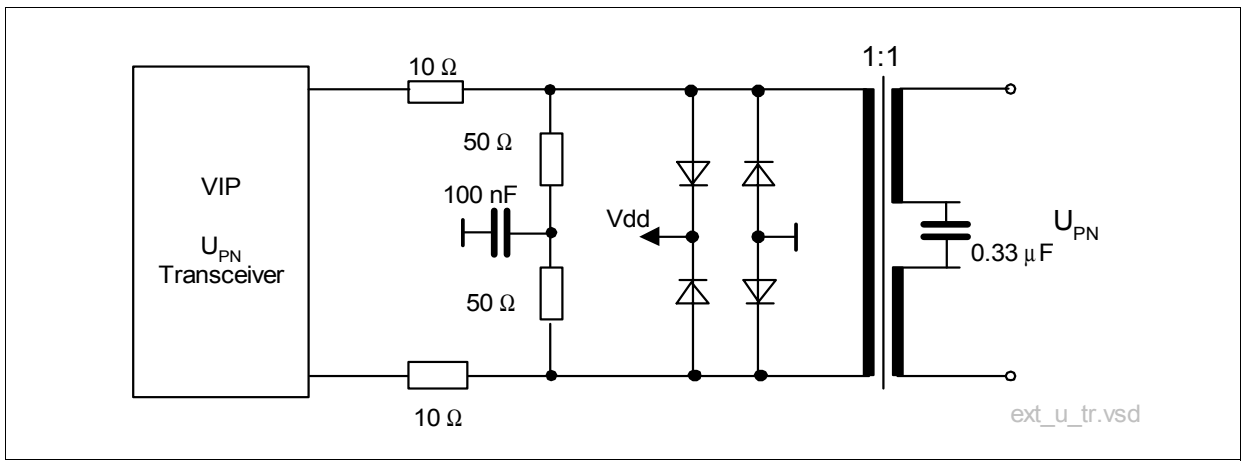


Figure 28 External Transceiver Circuitry of the VIP in U_{PN} Mode

*Note: The resistor values in **Figure 28** are optimized for an ideal transformer (R_{Cu} = 0). The 0.33-µF capacitance will be verified during system tests.*

6.1.3 S/T Interface External Circuitry

The VIP needs some external circuitry to achieve impedance matching, overvoltage protection and ElectroMagnetic Compatibility (EMC) for its connection to the 4-wire S/T interface. The configuration is shown in **Figure 29**.

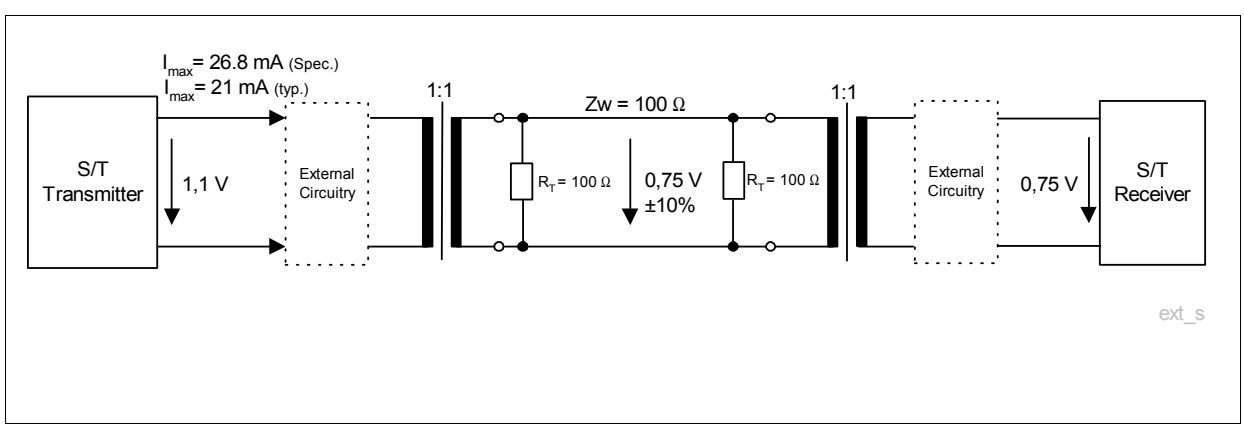


Figure 29 Overview of External Circuitry of the VIP in S/T Mode

Note: The actual values of the external resistors depend on the transformer selected. The resistor values are optimal for an ideal transformer (R_{Cu} = 0). Line termination (R_T) is usually applied to the NT and last wall outlet on the S bus only.

Transmitter. Dedicated external resistors (10 … 12.5 Ω) are required for the transmitter in order to

- Adjust the output voltage to the pulse mask (nominal 750 mV according to ITU-T I.430),
- Meet the output impedance of a minimum of 20 Ω (transmission of a binary '0' according to ITU-T I.430).

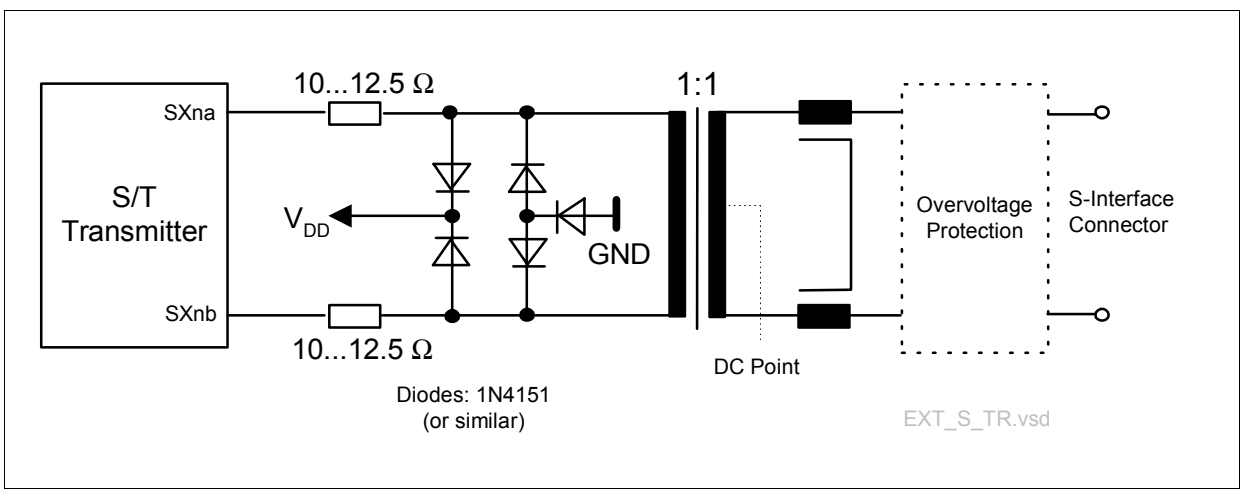


Figure 30 External S/T Transmitter Circuitry

Receiver. At the receiver, 8 kΩ overall resistance is needed in each receive path. It is recommended to use two resistors per line, as shown in **Figure 31**. This makes it possible to place a high resistance between the transformer and the diode protection circuit (required to pass 96-kHz input impedance test of ITU-T I.430). The remaining resistor protects the VIP receiver from input current peaks.

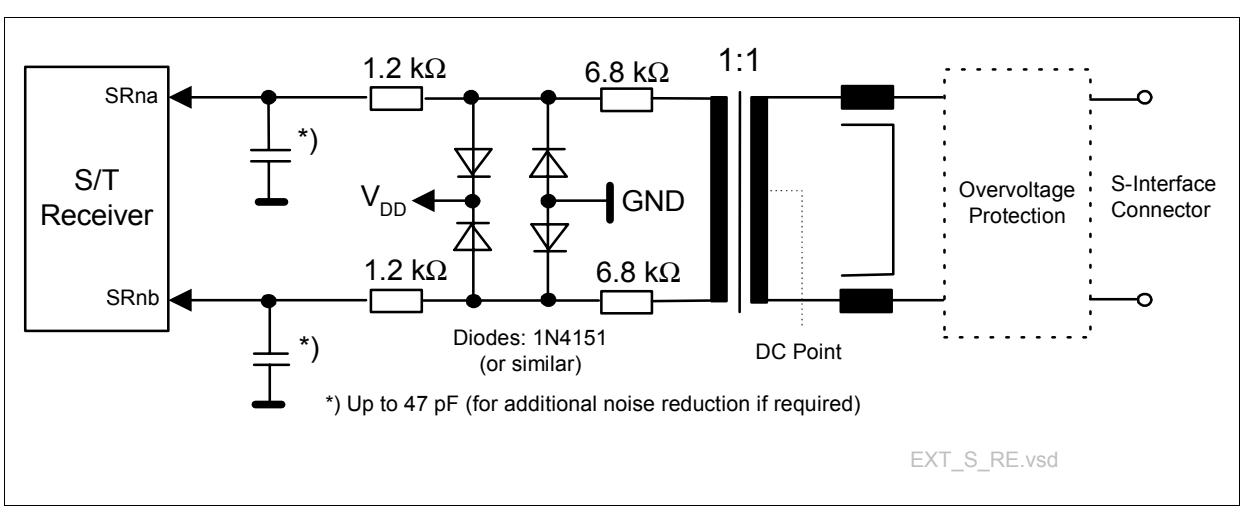


Figure 31 External S/T Receiver Circuitry

6.2 Wiring Configurations in LT-S Mode

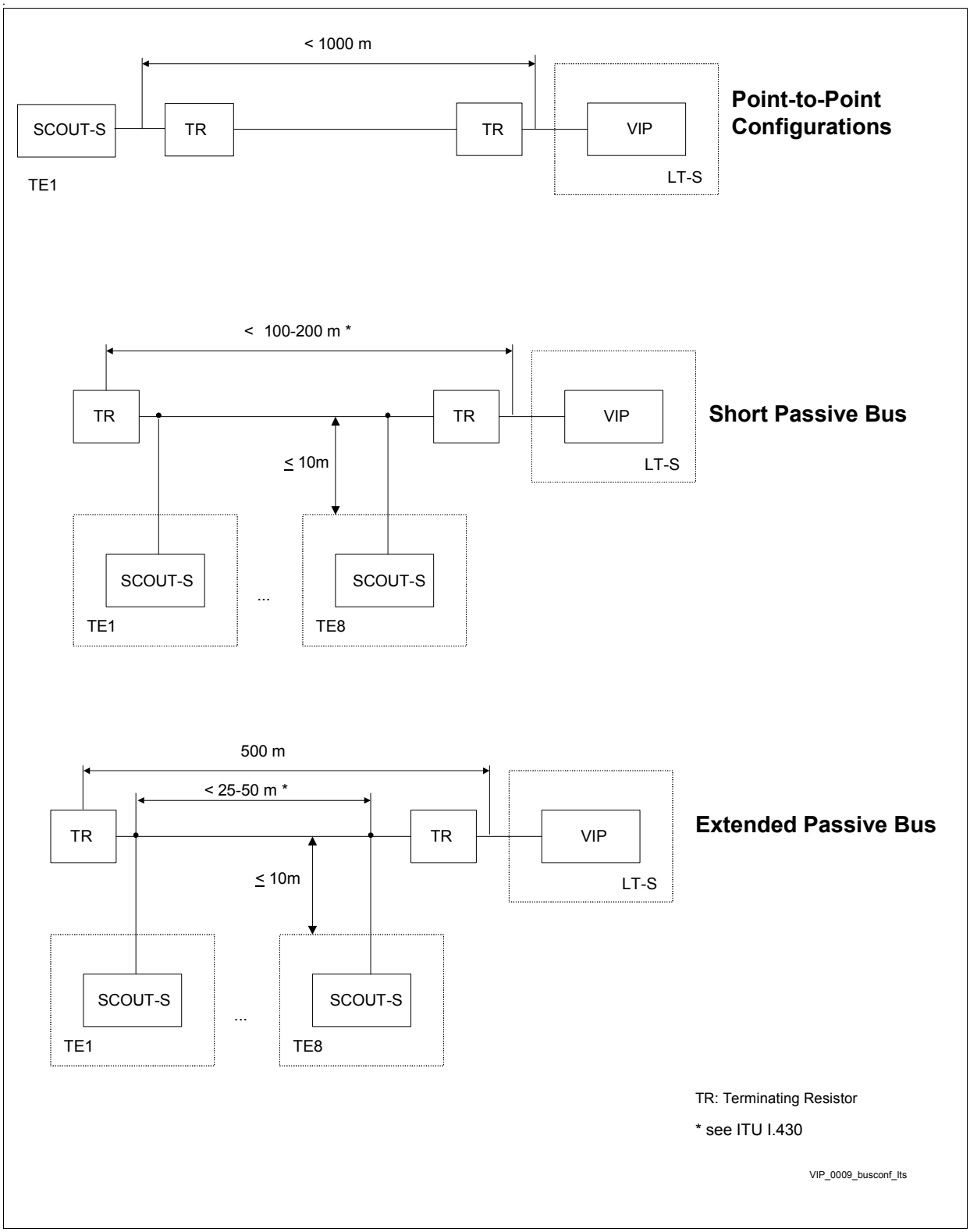


Figure 32 Wiring Configurations in User Premises (LT-S Mode)

6.3 Loop Modes

The following figure shows the different loops that can be closed in the VIP. Loops are programmed by the DELIC using the command bits LOOP, EXLP and TX_EN.

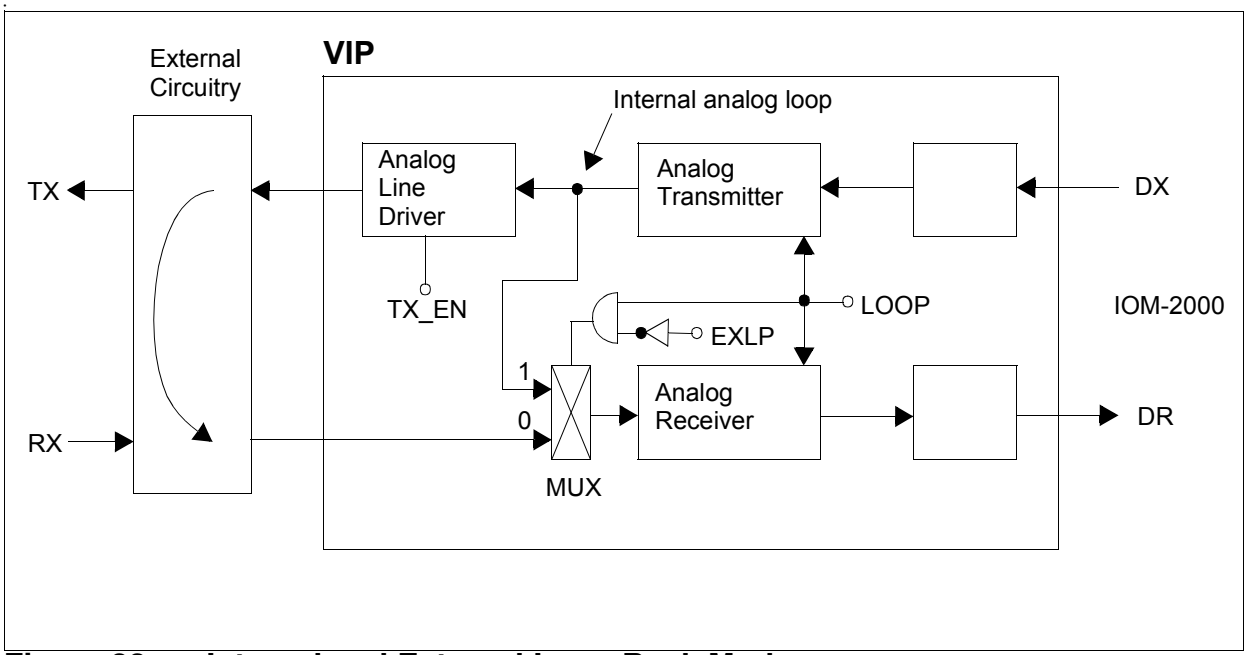
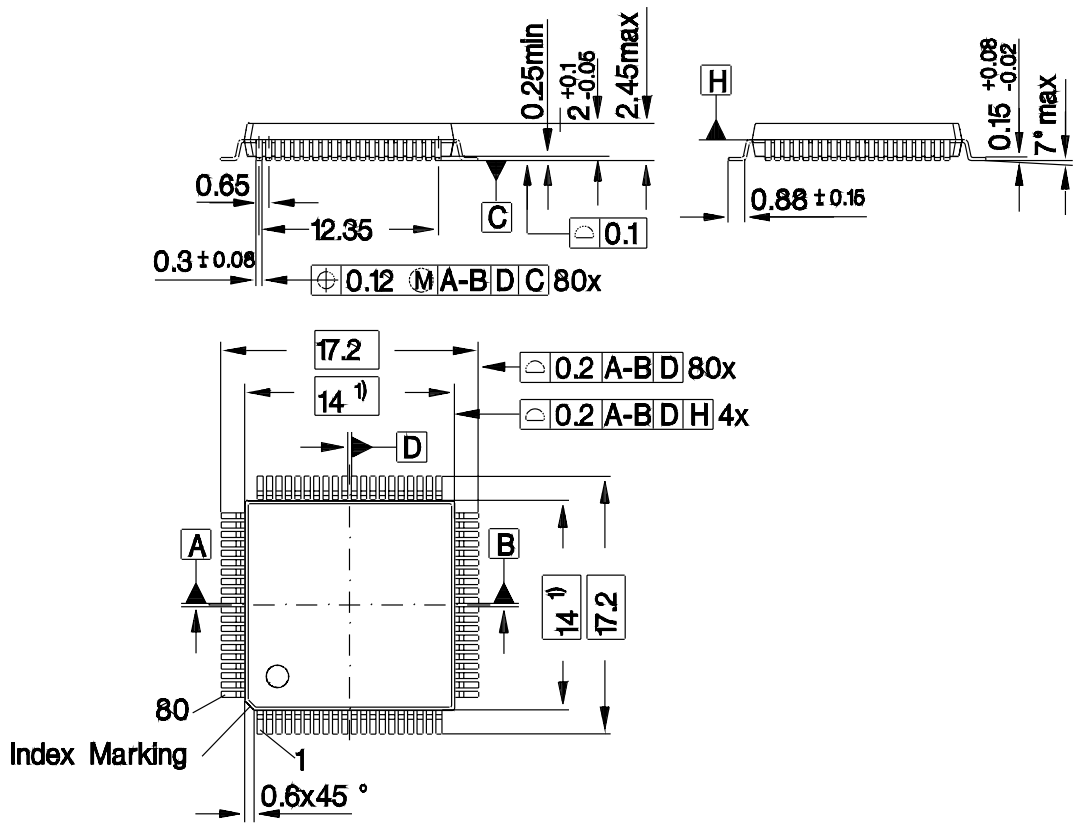


Figure 33 Internal and External Loop-Back Modes

7 Package Outlines

P-MQFP-80-1
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.
SMD = Surface Mounted Device

Dimensions in mm

8 Glossary

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AMI	Alternate Mark Inversion
ANSI	American National Standardization Institute
CMOS	Complementary Metal Oxide Semiconductor
CO	Central Office
DC	Direct Current
DECT	Digital European Cordless Telecommunication
DELIC	DSP Embedded Line and Port Interface Controller (PEB 20570, PEB 20571)
EMC	ElectroMagnetic Compatibility
ETSI	European Telephone Standards Institute
HDLC	High-level Data Link Control
IEEE	Institute of Electrical and Electronic Engineers
INFO	U- and S-interface signal as specified by ANSI/ETSI
I/O	Input/Output
IOM-2	ISDN-Oriented Modular 2nd generation
IOM-2000	Proprietary ISDN inferface for connection of VIP to DELIC
ISDN	Integrated services Digital Network
ITU	International Telecommunications Union
OCTAT-P	OCTAl Transceiver for U_{PN}-Interfaces (PEB 2096)
LT-S	Line Termination-Subscriber
LT-T	Line Termination-Trunk
PLL	Phase-Locked Loop
PBX	Private Branch Exchange
QUAT-S	QUAdrupleTransceiver for S/T-Interface (PEB 2084)
S/T	Two-wire pair interface
TAP	Test Access Port
U_{PN}	Two-wire interface
ZVEI	Zentralverband Elektrotechnik und Elektroindustrie e.V.

9 Index

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Dr. Ulrich Schumacher

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